Reliability Measurement of FPGA Implementations on Software-Defined Radio Platforms

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Reliability in Electronic Devices (hardware)
Parameters

(λ): Device's failure rate.

Failure In Time (FIT) rate: Number of failures that can be expected in 10^9 device-hours of operation.
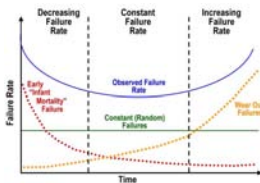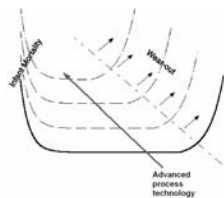

Figure: The Bathtub curve [1].

Figure: Evolution of the Bathtub curve.

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Reliability in Electronic Devices (hardware)
Parameters

Reliability ($R(t)$): The probability of an electronic system to perform its required functions under stated conditions for a specified period of time. $R(t_1)$ is the probability of a system will not fail in time t_1.

$$R(t) = e^{-\lambda t} \tag{1}$$

Mean Time Between Failures (MTBF): Average time a system runs between failure.

$$MTBF = \int_0^\infty e^{-\lambda t} dt = \frac{1}{\lambda} \tag{2}$$

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Reliability in Electronic Devices (hardware)
Temporal errors in electronic devices

Single Event Effects (SEEs):

1. Heavy ion strikes the silicon
2. It loses its energy via the production of free electron hole pairs
3. A dense ionized track in the local region is generated
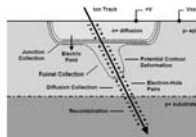4. A bit-flip can be induced (SEU, SET, SEFI, MBU, SEL -permanent-)

Figure: An ion passing through a transistor

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Reliability in Electronic Devices (hardware)
Fault tolerance techniques in electronic devices

Redundancy:

- **Physical redundancy:** Plain design, Tripe Modular Redundancy with simple voter, Partitioned Tripe Modular Redundancy with multiple simple voters, XTMR.

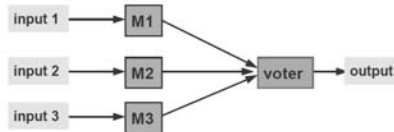- **Temporal redundancy:** Same processing $\Delta(t)$ and further comparison.

Figure: Tripe Modular Redundancy with simple voter.

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Reliability in Electronic Devices (hardware)
Standard for Functional Safety and Certifications

- Electronic products certification for critical applications
- Analysis and development methods
- Safety integrity levels: SIL1-SIL4 (IEC 61508)
- Two modes of operation: High demand rate and Low demand rate

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Reliability in Electronic Devices (hardware)
Safety integrity levels

Table: IEC-61508 Safety integrity Level for high demand rate systems
($dangerous failures/hr$)

Safety integrity Level	λ required
SIL4	between 10^{-8} and 10^{-9}
SIL3	between 10^{-7} and 10^{-8}
SIL2	between 10^{-6} and 10^{-7}
SIL1	between 10^{-5} and 10^{-6}

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Reliability in Electronic Devices (hardware)
FPGAs nowadays
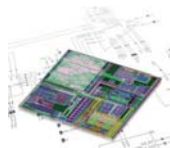COTS FPGAs on critical applications
FT and EM techniques in FPGAs

FPGAs nowadays
The electronic design is living a 'revolution'

Current status:

- New silicon technologies allow the integration of whole digital systems in a single 'chip'

- The design of Application Specific Integrated Circuits is more and more expensive, complex and risky

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FPGAs nowadays
Answer: **Reconfigurable logic (FPGAs)**

What is a FPGA?:

- It is similar to a 'un-formatted chip'
- It can be 'load' with a custom circuit designed using specific EDA tools
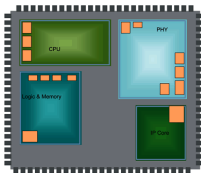- Modern FPGAs offer similar features to ASICs

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FPGAs nowadays
FPGAs trade-off

Success keys:

- Affordable engineering
- Low risk: Reconfigurable
- Low product *time-to-market*
- Flexible electronic boards (they can be reused for different products)

Challenges:

- Susceptible to SEE (SEUs)
- Programmability (Safety standards)

- Example:
  - Virtex-5 nominal 131 FIT/Mb configuration cells [2]
  - XC5VLX50T 11,37 Mb of configuration cells > 1489 FIT nominal or an MTBF of 77 years

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COTS FPGAs on critical applications
NASA SpaceCube (source [3])

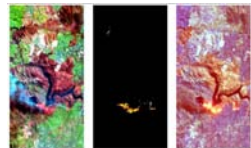

Figure: SPACE cube 1.0 CPU.

Figure: STS-125 launch.

Figure: California wildfire scene

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FT and EM techniques in FPGAs
Temporal errors in FPGAs

Figure: FPGA architecture.
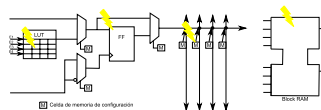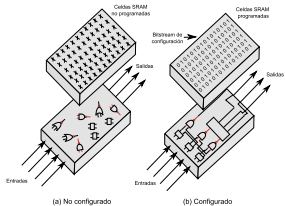
Figure: SEU effect in FPGAs.

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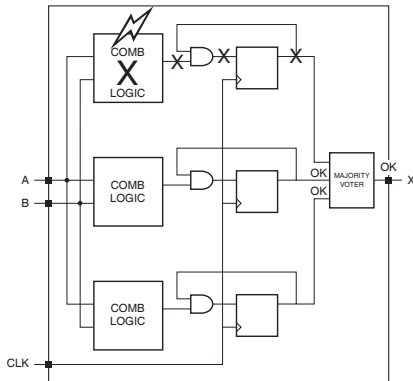
Figure: Tripe Modular Redundancy with simple voter in a FPGA. [4]

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FT and EM techniques in FPGAs

XTMR architecture - XTMR triplicates:

- **All inputs** including clocks and throughput (combinational) logic.

- **Feedback logic** and inserting majority voters on feedback paths.

- **All outputs**, using minority voters to detect and disable incorrect output paths.
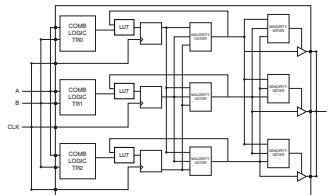
Figure: XTMR architecture.

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XTMR design flow:

Figure: XTMR design flow.

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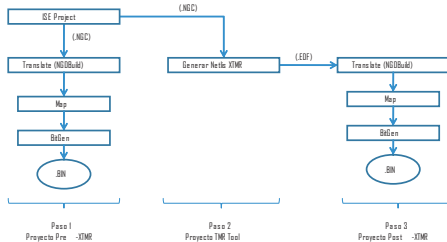
FT and EM techniques in FPGAs

Scrubbing:
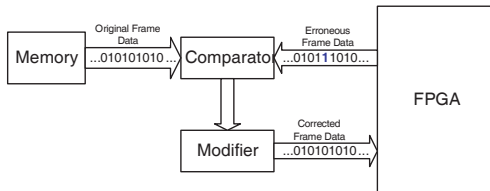
Figure: Scrubbing concept.

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FT and EM techniques in FPGAs

Internal Scrubbing combined with Error Correcting Code (ECC):
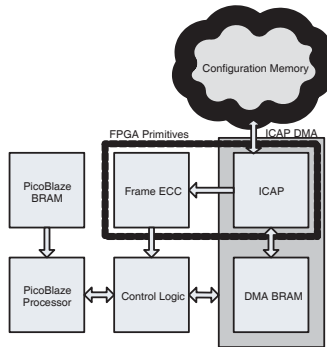
Figure: SEU controller macro in Virtex-5 [5].

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Block RAMs Scrubbing (Internal RAM memory):
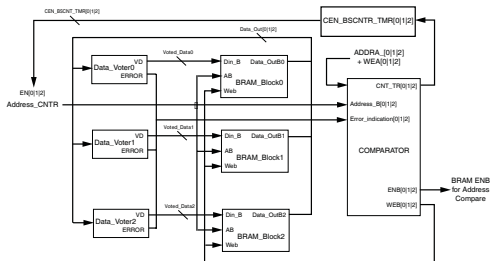
Figure: BlockRAM scrubber macro block diagram [6].

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Partial Reconfiguration for Fault Tolerance

- Partial reconfiguration is supported by Xilinx
- Technological challenges overcome (Virtex-4):
  - Internal reconfiguration ports (ICAP)
  - No frame restriction (16-CLB range)
  - No SRL16 and LUT RAMs limitations
- RPD Design flow enhanced
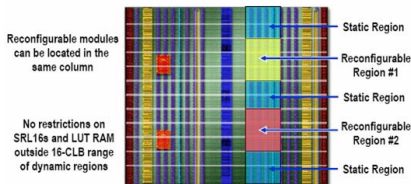
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SEU Test Set-up
Analysis Results for Cipher Blocks
Analysis Results for on-chip bus Architectures

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Analysis Results for Cipher Blocks
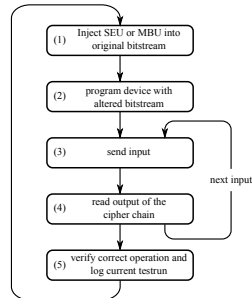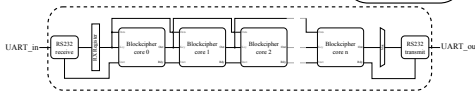Analysis Results for on-chip bus Architectures

SEU Test Set-up
Test Flow

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SEU Test Set-up
Analysis Results for Cipher Blocks
Analysis Results for on-chip bus Architectures
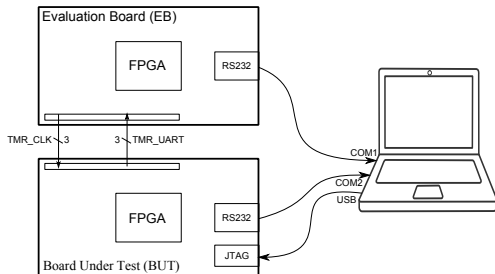
Analysis Results for Cipher Blocks
Test Flow

Analyzed SEU Resilience of the
following VHDL Cipher Blocks
[7]:

- DES [8]
- AES [9]
- Twofish [10]

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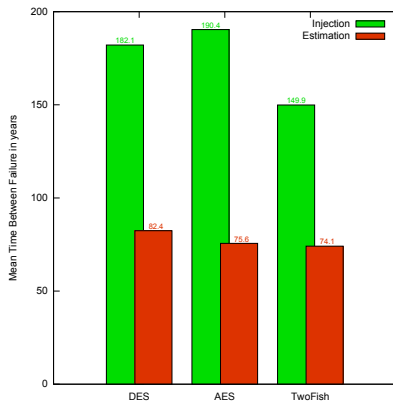
Analysis Results for on-chip bus Architectures
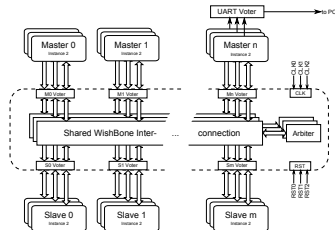## Redundant Architectures Compared
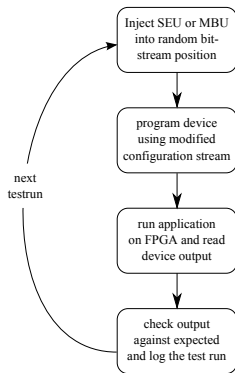
(a) Test Flow
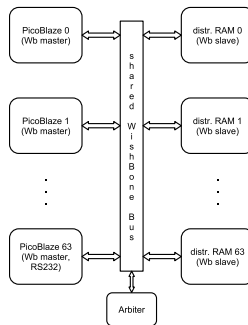
(b) Wishbone shared interconnection

[11]

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Analysis Results for on-chip bus Architectures
Redundant Architectures Compared
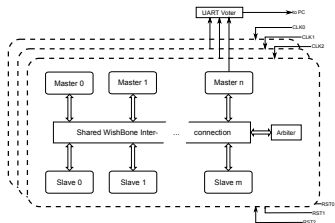
(c) Coarse-grained TMR

(d) Medium-grained TMR

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Analysis Results for on-chip bus Architectures
Analysis Results

Table: Test Results for External and Internal voting

Error type	Testruns	Coarse-grained		Medium-grained	
		Errors	Per-cent	Errors	Per-cent
SEU	17500	0	0	36	0.21
2bit-MBU	12500	58	0.46	51	0.41
2bit-MBU*	12500	36	0.29	67	0.54
3bit-MBU	12500	185	1.48	67	0.54
4bit-MBU	12500	337	2.70	103	0.82
5bit-MBU	12500	558	4.46	140	1.12

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Analysis Results

Table: Categories of test results

Cat.	Description	System behavior
A	All TMR layer counters are zero	Correct
B	One TMR layer counter differs from zero	
C	Two or three of the TMR layer counters differ from zero	
D	Two or three of the TMR layer counters differ from zero	Erroneous
E	Two or three of the TMR layer counters are zero	

APERT ☀SoC*e*
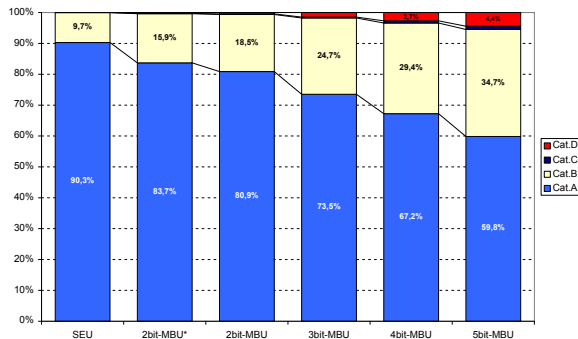
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Analysis Results

Partial Reconfiguration and TMR on FPGA based Rugged Systems

Safe*VPX* has 3U Eurocard size and it can run in stand-alone mode or it can be plugged in a 3U VPX (VITA 46, air-cooled) back-plane. In this last case, **Safe***VPX* supports 3 fat-pipes. Each fat-pipe is composed of four bidirectional Multi-Gigabit-Transceiver (MGT) links. Each fat-pipe channel allows the implementation of PCIe x4, Aurora or other protocol among high-speed communication standards.
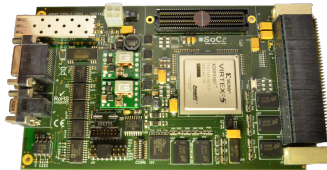
Key features

Features

- Virtex-5 FPGA (5VFX100-TFF1136) industrial range
- *Hard* PowerPC processor FPGA embedded
- CRC protected DDR2 memory (5 Gb)
- 2 isolated CAN communication channels
- 1 isolated serial communications link
- 3 isolated sigma-delta ADCs
- 1 SFP connector (Gigabit Ethernet or Fibre Optics)
- Ready for stand-alone or VPX racked operation
- 3U Eurocard factor form (3U VPX VITA 46)

- FMC connector (only available for stand-alone (operation mode)
- Multiple options for full and partial bitstreams storage
- Extended temperature range

FPGA ready for Xilinx X-TMR implementation:
- Triplicated clock inputs
- Triplicated CAN communication lines
- Triplicated serial communication lines
- Triplicated General Purpose I/Os

Combination with SDR boards
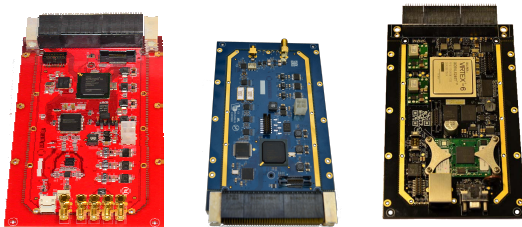
Rugged*SDR* Boards(VPX
or stand-alone)
Last generation
Software-Defined-
Radio boards for air
or conduction cooled
systems

Air-cool or Conduction-Cool

SDR*lab* **Chassis**
3U VPX Laboratory Equipment
with Power Supply and easily
removable cover

Light*VPX* **Chassis**
3U Conduction-cooled chassis and
clamshells

Conclusions

- Reliability in electronics systems is a challenge with nowadays levels of integration and complexity
- Modern FPGAs and SoPCs are the key circuits in state-of-the-art boards
- Error mitigation and Fault Tolerance traditional techniques are applicable with FPGAs
- Experimental analysis techniques combined with the use of standards defined for rugged systems can ensure high levels of reliability on SDR Platforms

Thank you for your attention!

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U. Kretzschmar, A. Astarloa, and J. Lázaro, "Seu resilience of des, aes and twofish in sram-based fpga," in *Reconfigurable Computing: Architectures, Tools and Applications.* Springer, 2013, pp. 37–46.

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U. Kretzschmar, A. Astarloa, J. Lazaro, M. Garay, and J. Del Ser, "Robustness of different tmr granularities in shared wishbone architectures on sram fpga," in *Reconfigurable Computing and FPGAs (ReConFig), 2012 International Conference on*, 2012, pp. 1–6.