SoC*e*

System-on-Chip *engineering*

User Guide for MEZU-*A7G8* Family

- Released -

Doc: 191010

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Revision History

Rev.	Date	Author	Description
191010	19/10/10	ES	Initial Version

Safety instructions

This chapter includes some instructions which must be observed to ensure your own personal safety and to avoid damage to devices and machinery.

Please observe the following warnings and recommendations:

- The device may only be employed for the purposes described in the user guide and technical description, and only in conjunction with external devices and components recommended or approved by **SoC***e* .
- The product can only be operated correctly and safely if it is transported, stored, installed and assembled properly and correctly. Furthermore, it must be operated and serviced carefully.
- This device is electrically operated. Adhere strictly to the safety requirements relating to voltages applied to the device.
- Beware of possible short circuits when connecting a cable section with conductive shielding braiding.
- Make sure that the electrical installation meets local or nationally applicable safety regulations.
- Never insert pointed objects (thin screwdrivers, wires, etc.) into the inside of the boards. Failure to observe this point may result in injuries caused by electric shocks.

Failure to observe the information given in these warnings could result in serious injury and/or major damage.

Only personnel that have received appropriate training should operate this device or work in its immediate vicinity. The personnel must be fully familiar with all of the warnings and maintenance measures in these operating instructions.

Correct transport, storage, and assembly as well as careful operation and maintenance are essential in ensuring safe and reliable operation of this device. Check whether the package was delivered complete and check the individual parts for transport damage.

Use only undamaged parts!

These products are only to be used in the manner indicated in this version of the user guide. Particular attention is to be paid to all warnings and items of information relating to safety.

Recycling Note

After its use, this product has to be processed as electronic scrap and disposed of according to the prevailing waste disposal regulations of your community / district / country / state.

Disclaimer Note

The performance features described here are binding only if they have been expressly guaranteed in the purchasing agreement. We have checked that the contents of the technical publication agree with the hardware and software described. However, it is not possible to rule out deviations completely, so we are unable to guarantee complete agreement. However, the details in the technical publication are checked regularly. Any corrections which prove necessary are contained in subsequent editions. We reserve the right to make technical modifications.

We would furthermore point out that for reasons of simplicity, these operating instructions cannot describe every conceivable problem associated with the use of this equipment. Should you require further information or should particular problems occur which are not treated in sufficient detail in the operating instructions, you can request the necessary information from **SoC***e* . You can find the contact details on the Internet: http://www.soc-e.com.

We are grateful for suggestions for improvement.

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1 Introduction

MEZU–*A7G8* is a pluggable module designed to enable easy integration of Ethernet Industrial Networks in equipments for Electric, Transportation, Aerospace and Industrial Automation sectors. This powerful module allows the implementation of custom switches or end-equipments with powerful networking capabilities. Network frame processing can be performed by hardware using specific IPs.
MEZU–*A7G8* base device is Artix-7 FPGA from Xilinx. Figures 1.1 and 2.2 show a block diagram and a top view of the **MEZU–***A7G8* respectively.

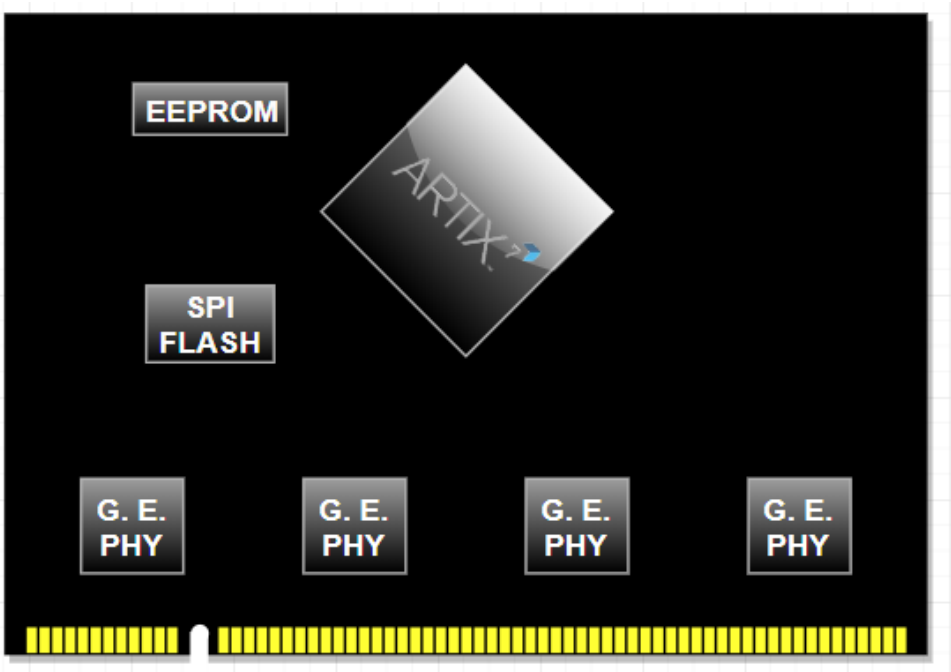

Figure 1.1: **MEZU–***A7G8* Block Diagram.

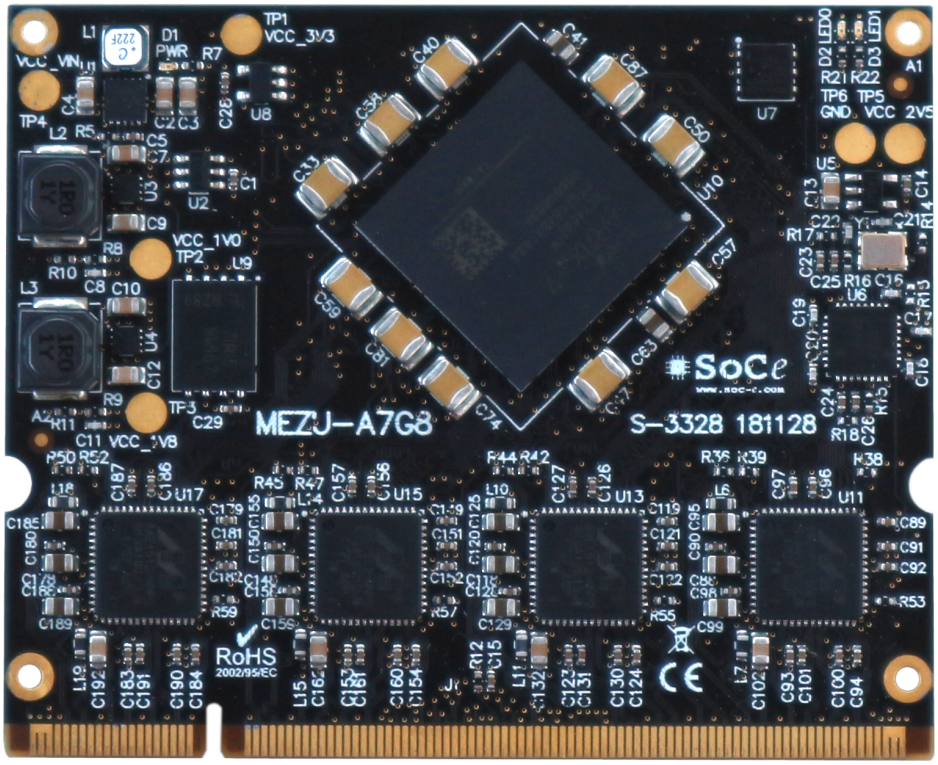

Figure 1.2: **MEZU–***A7G8* Top View.

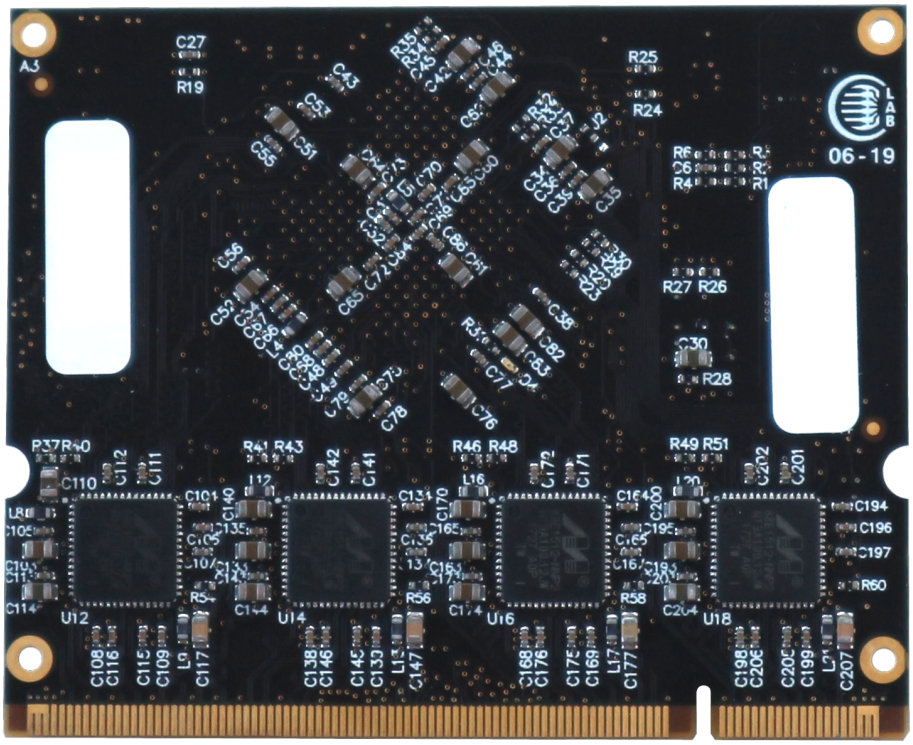

Figure 1.3: **MEZU–***A7G8* Bottom View.

MEZU–*A7G8* can be plugged on **MEZU–***carrier-A7G8* to form a **MEZU–***brick-A7G8* to develop custom Gigabit Ethernet designs with IPs such as HSR/PRP and IEEE 1588, and evaluate its performance. Figure 1.4 depicts a block diagram and a top view of the **MEZU–***carrier-A7G8* and Figure 1.5 shows an snapshot of the Top Side of this board:

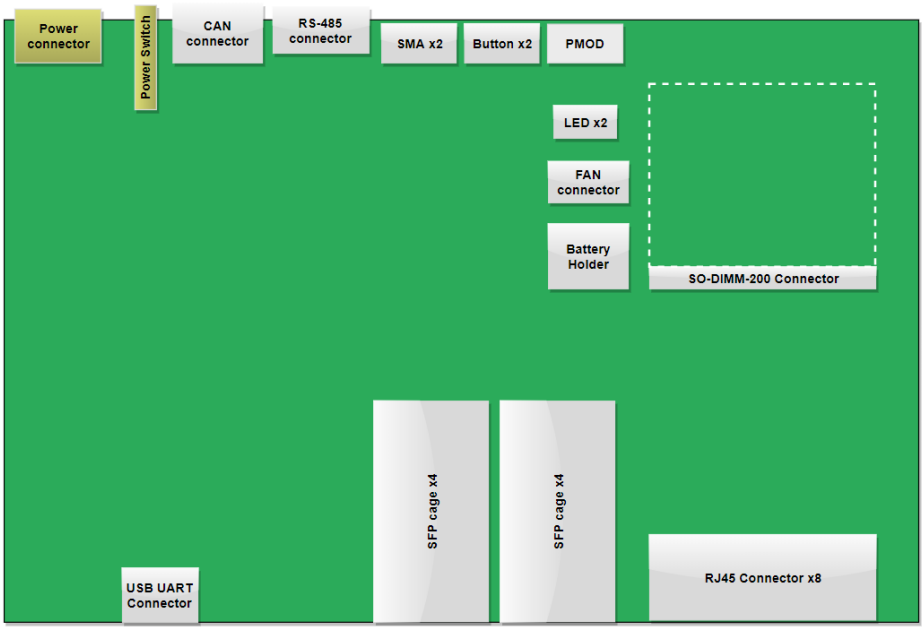

Figure 1.4: MEZU–carrier-A7G8 Block Diagram.

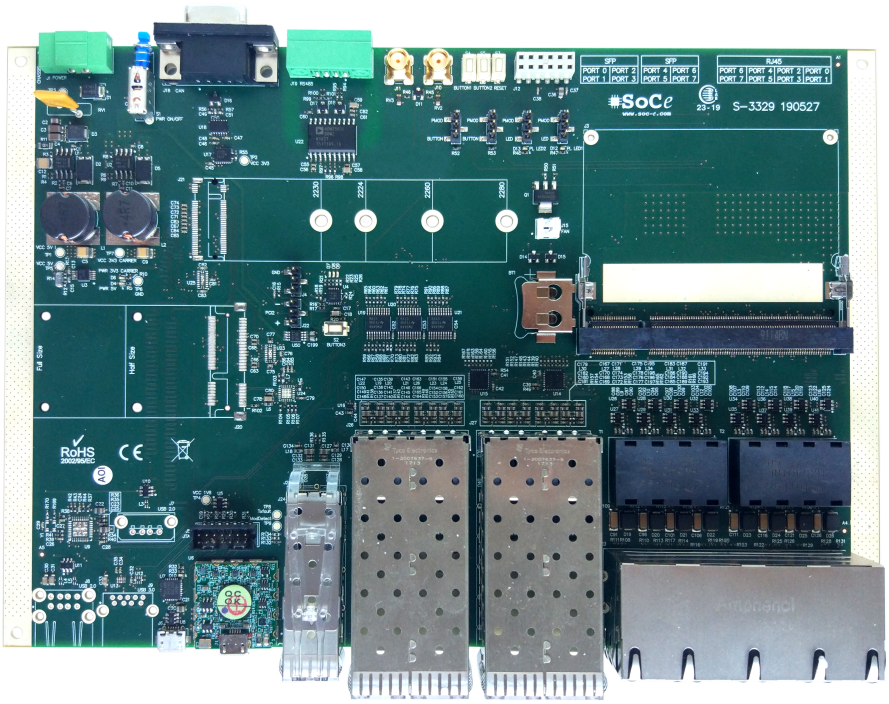

Figure 1.5: MEZU–carrier-A7G8 Top View.

2 MEZU–*A7G8* Family Functional description

2.1 MEZU–*A7G8*

This section presents the main components mounted on **MEZU–*A7G8***. The Block Diagram depicted on Figure 2.1 represents the approximate location of each device in the module.

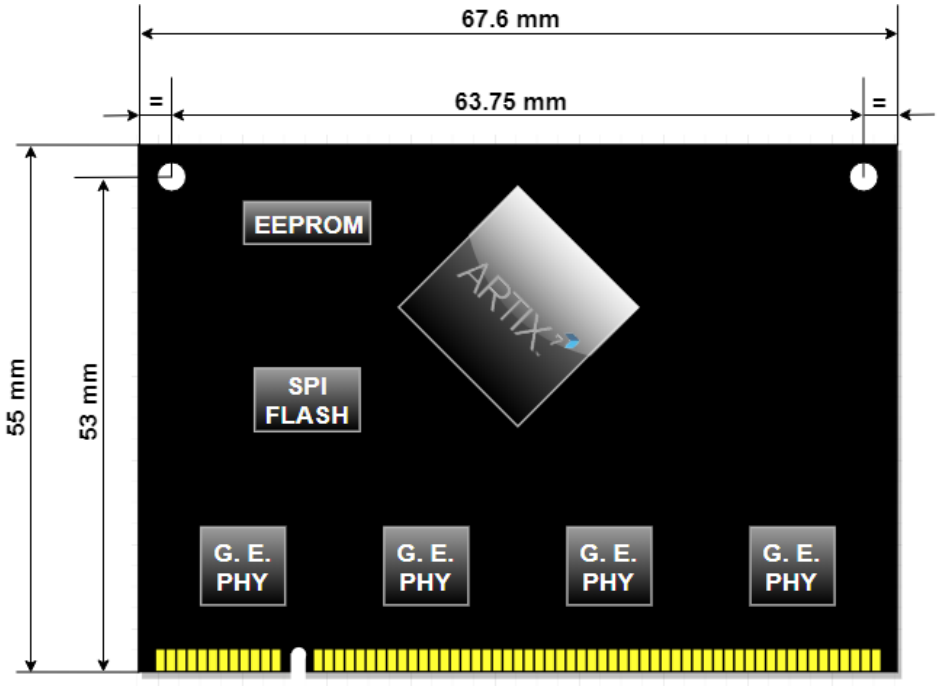

Figure 2.1: **MEZU–*A7G8*** Block Diagram.

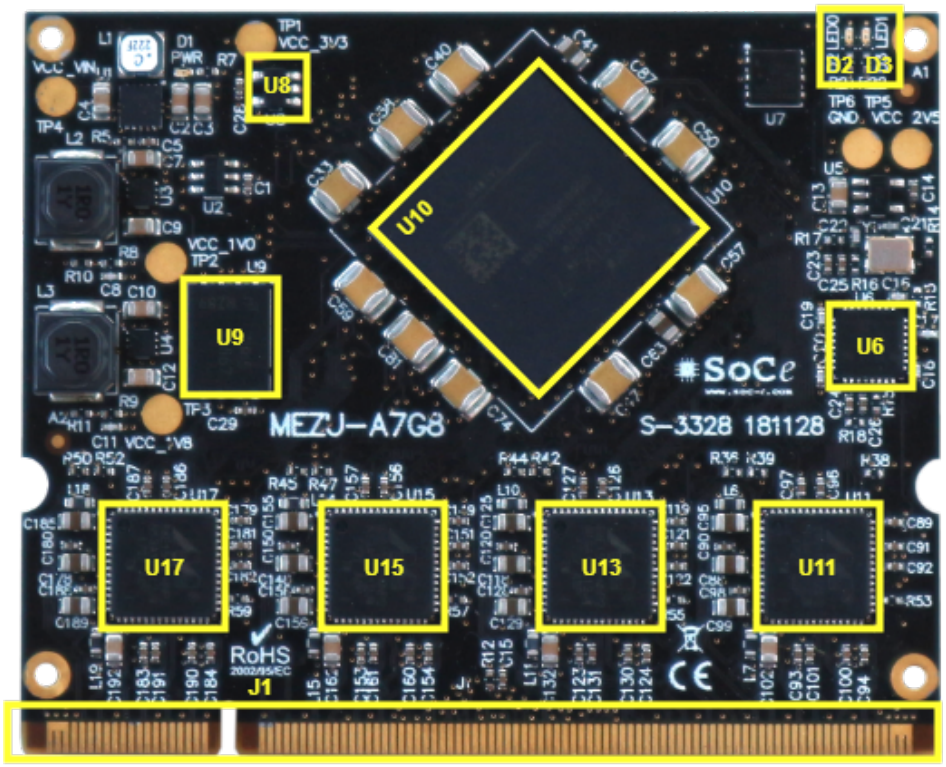

Figure 2.2: **MEZU–A7G8** Main Components.

2.1.1 Artix-7 FPGA (U10)

The main device populated on **MEZU–A7G8** is the Xilinx Artix-7 FPGA. XC7A100T-1FTG256I device is mounted on the standard version; also XC7A75T and XC7A50T devices can be mounted upon request.

Pinout

Table 2.1 summarizes the pin locations used on the Artix-7 and their correspondence with signals on the board.

Pin	Signal name	Pin	Signal name
Bank 14			
K12	PL_ETH6_RX_DV	N11	PL_SYS_CLK
J13	PL_FLASH_MOSI	N12	PL_ETH7_RX_CLK
J14	PL_FLASH_MISO	P10	PL_ETH7_TX_CLK
K15	PL_FLASH_WP_N	P11	PL_LED1
K16	PL_FLASH_HOLD_N	R12	PL_ETH7_RX_D2
L15	NC	T12	PL_ETH7_TX_D1
M15	PL_ETH6_RX_D3	R13	PL_ETH7_TX_D0

Pin	Signal name	Pin	Signal name
L14	PL_ETH6_RX_D2	T13	PL_ETH7_RX_DV
M14	PL_ETH6_RX_D0	R10	PL_ETH7_RX_D1
K13	PL_ETH6_TX_D0	R11	PL_ETH7_RX_D3
L13	PL_ETH6_RX_D1	N9	PL_ETH7_TX_EN
L12	PL_FLASH_CS_N	P9	PL_ETH7_TX_D2
M12	PL_LED0	M6	PL_ETH7_ACT
M16	PL_ETH6_TX_D1	N6	PL_ETH7_LINK
N16	PL_ETH6_TX_D2	P8	PL_ETH7_TX_D3
P15	PL_ETH6_TX_D3	R8	PL_ETH7_MDC_OEM
P16	PL_ETH6_TX_EN	T7	PL_GPIO_1V8_07
R15	PL_ETH6_MDC_OEM	T8	PL_GPIO_1V8_08
R16	PL_ETH6_MDIO_OEM	T9	PL_GPIO_1V8_06
T14	PL_ETH6_ACT	T10	PL_ETH7_RX_D0
T15	PL_ETH6_LINK	R5	PL_GPIO_1V8_04
N13	PL_ETH6_RX_CLK	T5	PL_GPIO_1V8_05
P13	PL_SYS_RST	R6	PL_GPIO_1V8_09
N14	PL_ETHX_RESET_NEG	R7	PL_GPIO_1V8_10
P14	PL_ETH6_TX_CLK	P6	PL_ETH7_MDIO_OEM
Bank 15			
D10	PL_ETH3_ACT	E12	PL_ETH5_TX_CLK
C8	PL_ETH3_MDC_OEM	E13	PL_ETH5_RX_CLK
C9	PL_ETH3_TX_D3	E11	PL_ETH4_MDC_OEM
A8	PL_ETH3_TX_EN	D11	PL_ETH3_TX_CLK
A9	PL_ETH3_TX_D1	D14	PL_ETH4_TX_D0
B9	PL_ETH3_TX_D2	D15	PL_ETH4_TX_EN
A10	PL_ETH3_RX_D3	F12	PL_ETH5_TX_EN
B10	PL_ETH3_TX_D0	F13	PL_ETH5_TX_D2
B11	PL_ETH3_RX_D2	E16	PL_GPIO_1V8_02
B12	PL_ETH3_RX_D0	D16	PL_GPIO_1V8_03
A12	PL_ETH3_RX_DV	F15	PL_ETH4_ACT
D8	PL_ETH3_MDIO_OEM	E15	PL_ETH4_MDIO_OEM
D9	PL_ETH3_LINK	H11	PL_ETH5_ACT
A13	PL_ETH4_RX_DV	G12	PL_ETH5_MDC_OEM
A14	PL_ETH4_RX_D0	H12	PL_ETH5_MDIO_OEM
C14	PL_ETH4_RX_D3	H13	PL_ETH5_TX_D3
B14	PL_ETH4_RX_D2	G14	PL_ETH5_TX_D1
B15	PL_ETH4_TX_D1	F14	PL_ETH4_LINK
A15	PL_ETH4_RX_D1	H16	PL_ETH5_RX_D2
C16	PL_ETH4_TX_D3	G16	PL_ETH5_RX_D3
B16	PL_ETH4_TX_D2	J15	PL_ETH5_RX_D0

Pin	Signal name	Pin	Signal name
C11	PL_ETH3_RX_CLK	J16	PL_ETH5_RX_D1
C12	PL_ETH3_RX_D1	H14	PL_ETH5_RX_DV
D13	PL_ETH4_TX_CLK	G15	PL_ETH5_TX_D0
C13	PL_ETH4_RX_CLK	G11	PL_ETH5_LINK
Bank 34			
L5	PL_ONE_WIRE	P3	PL_GPIO_3V3_05
L4	PL_GPIO_3V3_00	M5	PL_GPIO_3V3_06
M4	PL_GPIO_3V3_11	N4	PL_GPIO_3V3_07
M2	PL_GPIO_3V3_01	R2	PL_GPIO_3V3_08
M1	PL_GPIO_3V3_12	R1	PL_GPIO_3V3_09
N3	PL_GPIO_3V3_02	R3	PL_UART_TX_3V3
N2	PL_GPIO_3V3_13	T2	PL_UART_RX_3V3
N1	PL_GPIO_3V3_03	T4	PL_I2C_SCL_3V3
P1	PL_GPIO_3V3_14	T3	PL_I2C_SDA_3V3
P4	PL_GPIO_3V3_04	P5	PL_GPIO_3V3_10
Bank 35			
E6	PL_ETH1_RX_DV	F5	PL_ETH1_RX_D1
B7	PL_GPIO_1V8_00	E5	PL_ETH1_RX_D0
A7	PL_GPIO_1V8_01	F4	PL_ETH1_RX_CLK
B6	PL_ETH2_TX_EN	F3	PL_ETH1_TX_CLK
B5	PL_ETH2_TX_D3	F2	PL_ETH0_TX_D3
A5	PL_ETH2_TX_D2	E1	PL_ETH0_MDC_OEM
A4	PL_ETH2_TX_D0	G5	PL_ETH1_RX_D2
B4	PL_ETH2_TX_D1	G4	PL_ETH1_TX_D0
A3	PL_ETH2_RX_D2	G2	PL_ETH0_TX_D2
C7	PL_ETH2_MDC_OEM	G1	PL_ETH0_TX_D1
C6	PL_ETH2_MDIO_OEM	H5	PL_ETH1_RX_D3
D6	PL_ETH2_ACT	H4	PL_ETH1_TX_D1
D5	PL_ETH2_LINK	J5	PL_ETH1_MDC_OEM
C3	PL_ETH2_RX_D3	J4	PL_ETH1_TX_D2
C2	PL_ETH0_ACT	H2	PL_ETH0_TX_D0
B2	PL_ETH2_RX_D0	H1	PL_ETH0_RX_D3
A2	PL_ETH2_RX_D1	J3	PL_ETH1_TX_EN
C1	PL_ETH0_LINK	H3	PL_ETH1_TX_D3
B1	PL_ETH2_RX_DV	K1	PL_ETH0_RX_D1
E2	PL_ETH0_TX_EN	J1	PL_ETH0_RX_D2
D1	PL_ETH0_MDIO_OEM	L3	PL_ETH1_ACT
E3	PL_ETH0_RX_CLK	L2	PL_ETH0_RX_DV
D3	PL_ETH0_TX_CLK	K3	PL_ETH1_LINK
D4	PL_ETH2_RX_CLK	K2	PL_ETH0_RX_D0

Pin	Signal name	Pin	Signal name
C4	PL_ETH2_TX_CLK	K5	PL_ETH1_MDIO_OEM

Table 2.1: MEZU–A7G8 Artix-7 Pinout.

2.1.2 System clock (U6)

The FPGA has a dedicated 25 MHz clock input (N11, LVCMOS18) driven by a LMK00101 clock distributor chip. All PHYs share the same clock source managed by this chip as well.

2.1.3 SPI flash (U9)

MEZU–A7G8 features a 256 Mb Quad SPI Flash. The Micron MT25QU256ABA device is used on this board.
The Multi-I/O SPI Flash memory is used to provide non-volatile boot, application code, and data storage.
The relevant device attributes are:

- 256Mbit.
- x1, x2, and x4 support.
- Speeds up to 166 MHz.
- In Quad-SPI mode, this translates to 90MB/s.
- 1.7-2.0V single supply power.

2.1.4 EEPROM (U8)

MEZU–A7G8 features a 2 Kb I2C serial EEPROM with unique MAC. The Microchip 24AA02E48 device is used on this board. It can be used to store configuration values.

2.1.5 LEDs (D2, D3)

MEZU–A7G8 has 2x LED and can be used via GPIO of the FPGA.

2.1.6 GE PHY (U11, U12, U13, U14, U15, U16, U17, U18)

The MEZU–A7G8 includes 8x Ethernet PHYs Marvell 88E1512. These PHYs support RGMII to Copper/Fiber/SGMII with Auto-Media Detect, RGMII to Copper, RGMII to SGMII/Fiber, and SGMII to Copper.

2.1.7 SO-DIMM-200 DDR2 Connector (J1)

A SO-DIMM-200 Connector is used to attach the MEZU–A7G8 to the MEZU–carrier-A7G8 or to the customer´s carrier. The pinout correspondences for the Connector is summarized in Table 2.2:

Connector (J1)

Pin	Signal name	Pin	Signal name
1	VCC_VIN	2	VCC_VIN
3	VCC_VIN	4	VCC_VIN
5	VCC_VIN	6	VCC_VIN
7	GND	8	GND
9	PHY6_MDI0_P	10	PHY7_MDI0_P
11	PHY6_MDI0_N	12	PHY7_MDI0_N
13	PHY6_MDI1_P	14	PHY7_MDI1_P
15	PHY6_MDI1_N	16	PHY7_MDI1_N
17	GND	18	GND
19	PHY6_MDI2_P	20	PHY7_MDI2_P
21	PHY6_MDI2_N	22	PHY7_MDI2_N
23	PHY6_MDI3_P	24	PHY7_MDI3_P
25	PHY6_MDI3_N	26	PHY7_MDI3_N
27	GND	28	GND
29	PHY6_SGMII_OUT_P	30	PHY7_SGMII_OUT_P
31	PHY6_SGMII_OUT_N	32	PHY7_SGMII_OUT_N
33	GND	34	GND
35	PHY6_SGMII_IN_P	36	PHY7_SGMII_IN_P
37	PHY6_SGMII_IN_N	38	PHY7_SGMII_IN_N
39	GND	40	GND
41	GND	42	GND
43	PHY4_MDI0_P	44	PHY5_MDI0_P
45	PHY4_MDI0_N	46	PHY5_MDI0_N
47	PHY4_MDI1_P	48	PHY5_MDI1_P
49	PHY4_MDI1_N	50	PHY5_MDI1_N
51	GND	52	GND
53	PHY4_MDI2_P	54	PHY5_MDI2_P
55	PHY4_MDI2_N	56	PHY5_MDI2_N
57	PHY4_MDI3_P	58	PHY5_MDI3_P
59	PHY4_MDI3_N	60	PHY5_MDI3_N
61	GND	62	GND
63	PHY4_SGMII_OUT_P	64	PHY5_SGMII_OUT_P

Pin	Signal name	Pin	Signal name
65	PHY4_SGMII_OUT_N	66	PHY5_SGMII_OUT_N
67	GND	68	GND
69	PHY4_SGMII_IN_P	70	PHY5_SGMII_IN_P
71	PHY4_SGMII_IN_N	72	PHY5_SGMII_IN_N
73	GND	74	GND
75	VCC_3V3	76	VCC_3V3
77	PL_GPIO_3V3_00	78	PL_UART_TX_3V3
79	PL_GPIO_3V3_01	80	PL_UART_RX_3V3
81	PL_GPIO_3V3_02	82	PL_I2C_SDA_3V3
83	PL_GPIO_3V3_03	84	PL_I2C_SCL_3V3
85	PL_GPIO_3V3_04	86	PL_GPIO_3V3_10
87	PL_GPIO_3V3_05	88	PL_GPIO_3V3_11
89	PL_GPIO_3V3_06	90	PL_GPIO_3V3_12
91	PL_GPIO_3V3_07	92	PL_GPIO_3V3_13
93	PL_GPIO_3V3_08	94	PL_GPIO_3V3_14
95	PL_GPIO_3V3_09	96	NC
97	GND	98	GND
99	VCC_1V8	100	VCC_1V8
101	PWR_GOOD_OUT	102	FPGA_TMS
103	PWR_EN_IN	104	FPGA_TCK
105	FPGA_DONE_OUT	106	FPGA_TDO
107	RST_IN_NEG	108	FPGA_TDI
109	PL_GPIO_1V8_00	110	PL_GPIO_1V8_09
111	PL_GPIO_1V8_01	112	PL_GPIO_1V8_10
113	PL_GPIO_1V8_02	114	NC
115	PL_GPIO_1V8_03	116	NC
117	PL_GPIO_1V8_04	118	NC
119	PL_GPIO_1V8_05	120	NC
121	PL_GPIO_1V8_06	122	NC
123	PL_GPIO_1V8_07	124	NC
125	PL_GPIO_1V8_08	126	NC
127	GND	128	GND
129	PHY2_MDI0_P	130	PHY3_MDI0_P
131	PHY2_MDI0_N	132	PHY3_MDI0_N
133	PHY2_MDI1_P	134	PHY3_MDI1_P
135	PHY2_MDI1_N	136	PHY3_MDI1_N
137	GND	138	GND
139	PHY2_MDI2_P	140	PHY3_MDI2_P
141	PHY2_MDI2_N	142	PHY3_MDI2_N
143	PHY2_MDI3_P	144	PHY3_MDI3_P

Pin	Signal name	Pin	Signal name
145	PHY2_MDI3_N	146	PHY3_MDI3_N
147	GND	148	GND
149	PHY2_SGMII_OUT_P	150	PHY3_SGMII_OUT_P
151	PHY2_SGMII_OUT_N	152	PHY3_SGMII_OUT_N
153	GND	154	GND
155	PHY2_SGMII_IN_P	156	PHY3_SGMII_IN_P
157	PHY2_SGMII_IN_N	158	PHY3_SGMII_IN_N
159	GND	160	GND
161	PHY0_MDI0_P	162	PHY1_MDI0_P
163	PHY0_MDI0_N	164	PHY1_MDI0_N
165	PHY0_MDI1_P	166	PHY1_MDI1_P
167	PHY0_MDI1_N	168	PHY1_MDI1_N
169	GND	170	GND
171	PHY0_MDI2_P	172	PHY1_MDI2_P
173	PHY0_MDI2_N	174	PHY1_MDI2_N
175	PHY0_MDI3_P	176	PHY1_MDI3_P
177	PHY0_MDI3_N	178	PHY1_MDI3_N
179	GND	180	GND
181	PHY0_SGMII_OUT_P	182	PHY1_SGMII_OUT_P
183	PHY0_SGMII_OUT_N	184	PHY1_SGMII_OUT_N
185	GND	186	GND
187	PHY0_SGMII_IN_P	188	PHY1_SGMII_IN_P
189	PHY0_SGMII_IN_N	190	PHY1_SGMII_IN_N
191	GND	192	GND
193	VCC_BAT	194	VCC_BAT
195	VCC_VIN	196	VCC_VIN
197	VCC_VIN	198	VCC_VIN
199	VCC_VIN	200	VCC_VIN

Table 2.2: MEZU-A7G8 SO-DIMM-200 DDR2 Connector Pinout.

2.2 **MEZU–***carrier-A7G8*

This section presents the main components mounted on **MEZU–***carrier-A7G8* . The Block Diagram depicted on Figure 2.3 represents the approximate location of each device in the module.

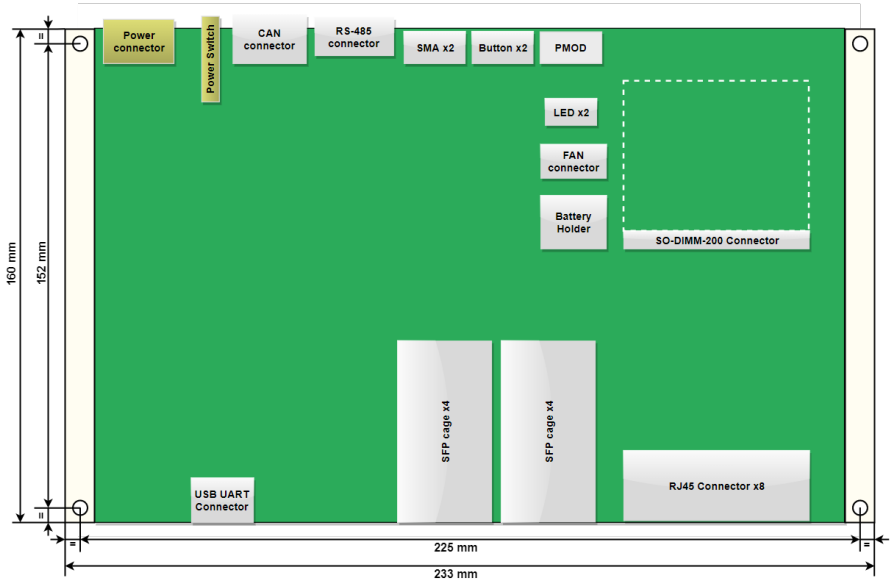

Figure 2.3: **MEZU–***carrier-A7G8* Block Diagram.

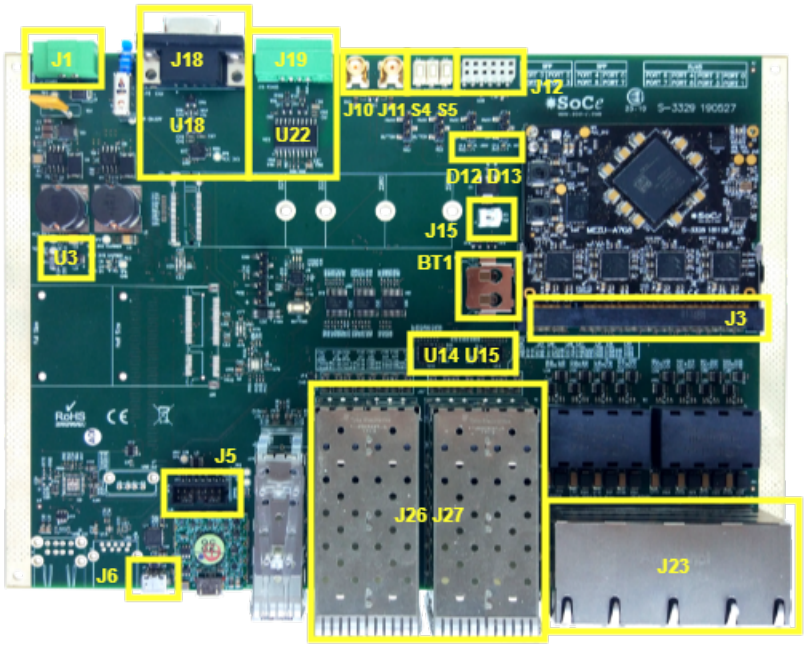

Figure 2.4: **MEZU–***brick-A7G8*.

2.2.1 USB to UART bridge (J6)

MEZU–*carrier-A7G8* has an integrated USB to UART bridge, with USB Female Micro-B type connector.

2.2.2 JTAG Connector (J5)

The **MEZU–***carrier-A7G8* has a JTAG connector to load and flash the **MEZU–***A7G8*.

2.2.3 Fan Connector (J15)

The **MEZU–***carrier-A7G8* has a two pin connector (640454-2) for 5V cooling fan. It is controlled via GPIO signals of the FPGA. The pinout of J15 is summarized in Table 2.3

Pin	Signal name
1	5V
2	GND

Table 2.3: **MEZU–***carrier-A7G8* Fan Connector Pinout.

2.2.4 Battery holder (BT1)

The **MEZU–***carrier-A7G8* has a LR44 battery holder to provide a limited backup supply. If used with **MEZU–***A7G8*, it provides support for bitstream encryption using BBRAM.

2.2.5 PMOD connector (J12)

The **MEZU–***carrier-A7G8* has a female PMOD standard compatible connector. This connector allows to connect several types of Digilent PMOD modules. The functionality of these PMODs is very wide, from simple push buttons to more complex modules like network interfaces, analog to digital converters, LCD displays or Bluetooth Modules.
Some GPIO signals for PMOD are shared with Buttons and LEDs. To route them to the PMOD, short with jumpers the position marked as PMOD on connectors J13, J14, J16 and J17.

2.2.6 Buttons (S4, S5)

The **MEZU–***carrier-A7G8* has 2x buttons and can be used via GPIO signals of the FPGA. The GPIO signals for buttons are share with PMOD. To route them to the buttons, short with jumpers the position marked as BUTTON on connectors J16 and J17.

2.2.7 LEDs (D12, D13)

The **MEZU–***carrier-A7G8* has 2x LED and can be used via GPIO signals of the FPGA.

The GPIO signals for LEDs are share with PMOD. To route them to the LEDs, short with jumpers the position marked as LED on connectors J13 and J14.

2.2.8 SMA connectors (J10, J11)

The **MEZU–***carrier-A7G8* has 2x SMA connectors and can be used via GPIO signals of the FPGA. This signals are shared with PMOD connector.

2.2.9 RS-485 (J19, U22)

The **MEZU–***carrier-A7G8* features the ADM2582E, an isolated RS-485 transceiver with a maximum data rate of 16Mbps. The connector (J19) mounted is 691382040004 from Wurth Electronics, and is wired as half-duplex. If full-duplex operation is desired, resistors R94 and R95 must be removed. The pinout of J19 is summarized in Table 2.4

Pin	Signal name	
	Full-duplex	**Half-duplex**
1	RS485_RX_P	RS485_RX_TX_P
2	RS485_RX_N	RS485_RX_TX_N
3	RS485_TX_P	RS485_RX_TX_P
4	RS485_TX_N	RS485_RX_TX_N

Table 2.4: **MEZU–***carrier-A7G8* RS-485 Connector Pinout.

2.2.10 CAN (J18, U18)

The **MEZU–***carrier-A7G8* has a high-speed CAN transceiver, the TJA1046. The transceiver is capable of reliable communication in the CAN FD fast phase at data rates up to 5 Mbps. The connector (J18) mounted is a female DB9. The pinout of J18 is summarized in Table 2.5

Pin	Signal name
1	NC
2	CANL
3	SIGNAL_GND
4	NC
5	CHASSIS_GND
6	SIGNAL_GND
7	CANH
8	NC
9	NC

Table 2.5: **MEZU–***carrier-A7G8* CAN Connector Pinout.

2.2.11 DC Input (J1)

The **MEZU–***carrier-A7G8* has a PHOENIX CONTACT 1817806 type (MC 1,5/ 2-GF-3,81-LR) DC connector (J1) onboard routed to two TPS54340 switching regulators (U1, U2).
The input voltage of the **MEZU–***carrier-A7G8* ranges from 5.5 V to 42 V (45 V Abs Max). In the **MEZU–***carrier-A7G8* configuration, U1 generates an output of 5V to power **MEZU–***A7G8*, and U2 generates 3.3V to power the **MEZU–***carrier-A7G8* .
The voltage rail for **MEZU–***A7G8* can be turned on and off with the S1 switch, and U2 is automatically controlled by a power good signal from **MEZU–***A7G8*.

2.2.12 I2C Power Monitor (U3)

The **MEZU–***carrier-A7G8* features an I2C current and power monitor, the INA226, which is connected to the I2C bus of **MEZU–***A7G8* (See 2.1) through the SO-DIMM-200 connector (See 2.6)

2.2.13 I2C IO Expander (U14, U15)

MEZU–*carrier-A7G8* uses the TI TCA6424A low voltage I2C 24-bit I/O expander device to control the LEDs of RJ45 and SFP ports, and also the LOS signals of the SFP ports. The I2C 24-bit I/O expander device is connected to the I2C bus of **MEZU–***A7G8* (See 2.1) through the SO-DIMM-200 connector (See 2.6).

2.2.14 RJ-45 Gigabit Ethernet Connectors (J23)

The **MEZU–***carrier-A7G8* includes 8 RJ45 Gigabit Ethernet connectors. Their differential signals are routed to **MEZU–***A7G8*'s PHYs through the SO-DIMM-200 connector (See 2.6).

2.2.15 SFP cages (J26, J27)

The **MEZU–***carrier-A7G8* mounts 8 SFP Cages. Their RX and TX differential signals are routed to the SO-DIMM-200 connector and links with the Gigabit PHYs as specified in Table 2.6.

2.2.16 SO-DIMM-200 Connector (J3)

MEZU–*carrier-A7G8* features a SO-DIMM-200 slot to connect to **MEZU–***A7G8* or to the customer´s module. The pinout correspondences for Connector is summarized in Table 2.6:

Connector (J3)

Pin	Signal name	Pin	Signal name
1	VCC_VIN	2	VCC_VIN
3	VCC_VIN	4	VCC_VIN
5	VCC_VIN	6	VCC_VIN
7	GND	8	GND
9	PHY6_MDI0_P	10	PHY7_MDI0_P
11	PHY6_MDI0_N	12	PHY7_MDI0_N
13	PHY6_MDI1_P	14	PHY7_MDI1_P
15	PHY6_MDI1_N	16	PHY7_MDI1_N
17	GND	18	GND
19	PHY6_MDI2_P	20	PHY7_MDI2_P
21	PHY6_MDI2_N	22	PHY7_MDI2_N
23	PHY6_MDI3_P	24	PHY7_MDI3_P
25	PHY6_MDI3_N	26	PHY7_MDI3_N
27	GND	28	GND
29	PHY6_SGMII_OUT_P	30	PHY7_SGMII_OUT_P
31	PHY6_SGMII_OUT_N	32	PHY7_SGMII_OUT_N
33	GND	34	GND
35	PHY6_SGMII_IN_P	36	PHY7_SGMII_IN_P
37	PHY6_SGMII_IN_N	38	PHY7_SGMII_IN_N
39	GND	40	GND
41	GND	42	GND
43	PHY4_MDI0_P	44	PHY5_MDI0_P
45	PHY4_MDI0_N	46	PHY5_MDI0_N
47	PHY4_MDI1_P	48	PHY5_MDI1_P
49	PHY4_MDI1_N	50	PHY5_MDI1_N
51	GND	52	GND
53	PHY4_MDI2_P	54	PHY5_MDI2_P
55	PHY4_MDI2_N	56	PHY5_MDI2_N
57	PHY4_MDI3_P	58	PHY5_MDI3_P
59	PHY4_MDI3_N	60	PHY5_MDI3_N
61	GND	62	GND
63	PHY4_SGMII_OUT_P	64	PHY5_SGMII_OUT_P
65	PHY4_SGMII_OUT_N	66	PHY5_SGMII_OUT_N
67	GND	68	GND
69	PHY4_SGMII_IN_P	70	PHY5_SGMII_IN_P
71	PHY4_SGMII_IN_N	72	PHY5_SGMII_IN_N
73	GND	74	GND
75	VCC_3V3	76	VCC_3V3
77	RS485_RX	78	PL_UART_TX_3V3
79	RS485_TX	80	PL_UART_RX_3V3

Pin	Signal name	Pin	Signal name
81	RS485_nRE	82	PL_I2C_SDA_3V3
83	RS485_DE	84	PL_I2C_SCL_3V3
85	SMA_J10/PMOD	86	BUTTON_2/PMOD
87	SMA_J11/PMOD	88	LED_1/PMOD
89	CAN_TXD	90	LED_2/PMOD
91	CAN_RXD	92	PMOD
93	CAN_STB	94	FAN
95	BUTTON_1/PMOD	96	NC
97	GND	98	GND
99	VCC_1V8	100	VCC_1V8
101	PWR_GOOD_OUT	102	FPGA_TMS
103	PWR_EN_IN	104	FPGA_TCK
105	FPGA_DONE_OUT	106	FPGA_TDO
107	RST_IN_NEG	108	FPGA_TDI
109	NC	110	NC
111	NC	112	NC
113	NC	114	NC
115	NC	116	NC
117	NC	118	NC
119	NC	120	NC
121	NC	122	NC
123	NC	124	NC
125	NC	126	NC
127	GND	128	GND
129	PHY2_MDI0_P	130	PHY3_MDI0_P
131	PHY2_MDI0_N	132	PHY3_MDI0_N
133	PHY2_MDI1_P	134	PHY3_MDI1_P
135	PHY2_MDI1_N	136	PHY3_MDI1_N
137	GND	138	GND
139	PHY2_MDI2_P	140	PHY3_MDI2_P
141	PHY2_MDI2_N	142	PHY3_MDI2_N
143	PHY2_MDI3_P	144	PHY3_MDI3_P
145	PHY2_MDI3_N	146	PHY3_MDI3_N
147	GND	148	GND
149	PHY2_SGMII_OUT_P	150	PHY3_SGMII_OUT_P
151	PHY2_SGMII_OUT_N	152	PHY3_SGMII_OUT_N
153	GND	154	GND
155	PHY2_SGMII_IN_P	156	PHY3_SGMII_IN_P
157	PHY2_SGMII_IN_N	158	PHY3_SGMII_IN_N
159	GND	160	GND

Pin	Signal name	Pin	Signal name
161	PHY0_MDI0_P	162	PHY1_MDI0_P
163	PHY0_MDI0_N	164	PHY1_MDI0_N
165	PHY0_MDI1_P	166	PHY1_MDI1_P
167	PHY0_MDI1_N	168	PHY1_MDI1_N
169	GND	170	GND
171	PHY0_MDI2_P	172	PHY1_MDI2_P
173	PHY0_MDI2_N	174	PHY1_MDI2_N
175	PHY0_MDI3_P	176	PHY1_MDI3_P
177	PHY0_MDI3_N	178	PHY1_MDI3_N
179	GND	180	GND
181	PHY0_SGMII_OUT_P	182	PHY1_SGMII_OUT_P
183	PHY0_SGMII_OUT_N	184	PHY1_SGMII_OUT_N
185	GND	186	GND
187	PHY0_SGMII_IN_P	188	PHY1_SGMII_IN_P
189	PHY0_SGMII_IN_N	190	PHY1_SGMII_IN_N
191	GND	192	GND
193	VCC_BAT	194	VCC_BAT
195	VCC_VIN	196	VCC_VIN
197	VCC_VIN	198	VCC_VIN
199	VCC_VIN	200	VCC_VIN

Table 2.6: MEZU-carrier-A7G8 SO-DIMM-200 DDR2 Connector Pinout.