
SoCe
System-on-Chip engineering
Timing,
Networking
& Security


The global digitalization is
generating new challenges
that need to be faced

Boosting the digitalization of Critical Systems

When System-on-Chip engineering SL was founded in 2010, a strategy to evolve from a technology-based company to a customer-centric company was defined. This envision has helped us to succeed on selecting the right solutions to invest on and reaching outstanding customers world-wide.

Nowadays, the convergence on Ethernet is multisectoral. Industry, Energy, Automotive, Telecommunications and Aerospace are adopting massively interoperable Ethernet based solutions for their OT and IT networks. However, the original concept of Ethernet as a simple LAN network, has evolved to support real-time traffic, redundancy, high-data throughput and sophisticated cybersecurity mechanisms.

In this context of the "new" Ethernet, SoC-e know-how and technology have enabled the development of a broad range of Silicon IP and SoM solutions to reduce the time-to-market and design risks in hundreds of projects.

As an example, the Power Substation protections of the most relevant manufacturers implement our IP solution for high-availability Ethernet. Industrial PLCs and Industrial Networking equipment embed SoC-e time-aware Ethernet technology. Autonomous vehicle Lidars benefit from our unique CPU-less solution for nano-second range technology and, our comprehensive solution for Time-Sensitive Networking is already present in Railway, Industry 4.0 Factories and in Aerospace products and projects.

However, the global digitalization is generating new challenges that need to be faced. FPGA accelerated algorithms running on-premises and in Cloud servers enable re-thinking how to virtualize the Automation in the Factories and in Smart-Grid. Providing the best solutions for our customer´s need for high-data bandwidth, deterministic, secure and deep-packet analyzed Ethernet solution is our next goal. These new challenges for the Industrial and Aerospace sectors invite us to be pioneers once again and we will be glad to share this vision with you.

The SoCe Team

Technology

The benefits of the new generation Ethernet on Mission-Critical systems

High-reliability and availability in Industry, Automotive, Railway and Aerospace systems are a must. However, the current trend of OT/IT integration makes these systems more complex and vulnerable. These smarter infrastructures based on hyper-connected devices with sensing, processing and networking capabilities generate an incredible amount of data. Therefore, these sectors require standardized, interoperable and field-proven networking solutions. The proposed technologies shall at one hand, ensure that the real-time and critical-mission messages are transferred within strict bounds of latency and reliability and on the other, simplify the network infrastructure and operation.

In this sense, a multi-sectorial and world-wide agreed solution is the new generation Ethernet, named Time-Sensitive Networking. TSN delivers the traffic guaranteeing bandwidth and deterministic latency over Ethernet. The final aim is providing an unique network for real-time OT traffic and for high-bandwidth IT one.

SoC-e is providing a field-proven TSN technology to customers of critical-systems. The targeted equipment varies from small smart devices, CPUs or PLCs provided with few networking ports, up to multi-port Industrial Switches for the new generation factories. Additionally, a significative effort is being done in the field of contributing to the maturity and diffusion of this technology thanks to SoC-e kits and its continuous presence in the Interoperability events.

TSN comprises several standards. Currently, there are nine of them fully published and stable. The combination of features defined in them allows defining specific solutions for each sector. Indeed, there are multiple initiatives to define specific profiles for Industry, Automotive, 5G and others. Regarding the specific needs for Mission-Critical Systems, it worth to mention that TSN already includes means to support redundancy as defined in IEEE Std 802.1CB-2017. One of SoC-e technology key differentiation is the support for high-availability networking. Therefore, it is a pioneer technology provider offering this key feature in its TSN solutions portfolio. In addition to this zero-frames lost TSN, SoC-e offers high-availability alternatives based on other protocols like HSR, PRP, MRP or (M)RTSP.

One of the "hidden" features that is driving this evolution is the capability to synchronize systems and equipment in the range of nanosecond. Thanks to combined hardware and software implementations it is feasible distributing accurate timing over Ethernet networks. This time reference is the key to implement Deterministic Ethernet

and to share GPS-level precisions to 5G, Finance or Military systems using the wired infrastructure. This innovation offers an evident significative cost and complexity reduction and it allows proposing new services and products. From the technology point of view, the driver of this evolution is again an open and standardized protocol, the IEEE 1588 Precision Time Protocol. SoC-e portfolio includes all the elements needed to implement any PTP device, both hardware and software.

Once the technology of a unified network backbone for OT/IT is a reality, the interest on benefiting from aggregating intensive computation on Edge, FOG, on-premises or Cloud is a very active trend. Image & pattern recognition, machine learning, big-data analysis and security applications are only examples of fields where nowadays there are several R&D and business on-going initiatives. The SoC-e expertise on deep-packet analysis based on FPGA technology has been used to offer to the Electric Sector an IP solution offered as-a-service that accelerates the processing of the real time streams used to monitor the grid multiple orders of magnitude faster compared to traditional solutions.

In the field of Mission-Critical systems, the whole picture of digitalization is completed taking into account the security. Two key challenges in this context are the capability of upgrading securely and securing real-time traffic. In this catalog, solutions to secure at wire speed real time traffic and to upgrade securely FPGA system are presented. These hardware modules are completed with a software stack that implements security keys and certificates exchange mechanism as it is being defined by IEC.

1G Multiport TSN Switch

Time-Sensitive Networking (TSN) is an IEEE standardized solution that allows merging Real-Time traffic with Best-Effort one in a single Ethernet Network. TSN ensures delivering streams with guaranteed bandwidth and deterministic latency.

SoC-e's TSN solution is called **Multiport-TSN Switch (MTSN) IP**. It can be implemented optimally depending on the requirements of the final product, from a simple one port unit to a complex multiport switch. As an example, designs with requirements for TSN end-point, bridged end-point or multiport-gateway projects can be generated using MTSN switch IP. This IP can be easily implemented on reconfigurable SoCs. As an example, targeted devices are Xilinx Zynq Ultrascale+ MPSoC family. The IP includes Hardware and Software packages.

The designer can select, among other parameters, the number of ports and the TSN features for the switch implemented in the FPGA section. This tailored configuration can be done graphically using the GUI supported by Xilinx Vivado Tool IPI.

Key Features:

Interfaces:

- Full-duplex 10/100/1000 Mbps Ethernet
- Half-duplex 10/100 Mbps Ethernet Interfaces
- MII/RMII/GMII/RGMII/SGMII/QSGMII Physical Layer device (PHY) interfaces
- Copper and Fiber-optic media interfaces: 10/100/1000Base-T, 100Base-FX, 1000Base-X

Switching

- Non-blocking matrix architecture: 100% data throughput for GbE traffic
- Configurable from 1 up to 32 Ethernet ports
- Traffic Type Supported: Scheduled traffic, Best-effort Traffic and Reserved Traffic
- Time Aware Shaper: Configurable number and size of time slots
- Credit Based Shaper: Configurable bandwidth reservation for each traffic class
- Fast frame forwarding (cut-through) support between predefined port pairs
- Jumbo Frame support

Traffic Management

- Shared Dynamic and Static MAC Table (configurable size).
- Independent VLAN Learning support.
- Multicast Frame Filtering
- Switching Portmask: User-defined forwarding of frames to concrete ports
- Port-based VLAN switching
- Priorities (PCP-802.1p, DSCP TOS, Ethertype)
- DSA (Distributed Switching Architecture) tagging
- IGMPv2 snooping

Timing and TSN specific features

- IEEE 802.1AS(rev) for Time Synchronization Layer
- IEEE 802.1Qav for Reserved Traffic
- IEEE 802.1Qbv for Scheduled Traffic
- IEEE 802.1CB for Frame Replication and Elimination for Reliability
- IEEE 802.1Qcc for Network Management
- IEEE 802.1Qci for Stream Filtering and Policing
- IEEE 802.1AB for LLDP (Link Layer Discovery Protocol)
- IEEE 802.1w for Rapid Spanning Tree Protocol
- IEEE 802.1s for Multiple Spanning Tree Protocol
- Cut-Through support for Isochronous Scheduled Traffic
- IEEE 802.1Qat for Stream Reservation Protocol
- IEEE 802.1Qbu/802.3br for Frame Preemption

Security

- Per-Port Rate limiting (Broadcast, Multicast and Unicast traffic)
- Broadcast Storm Protection
- Port Mirroring: Ingress and/or egress traffic to any port

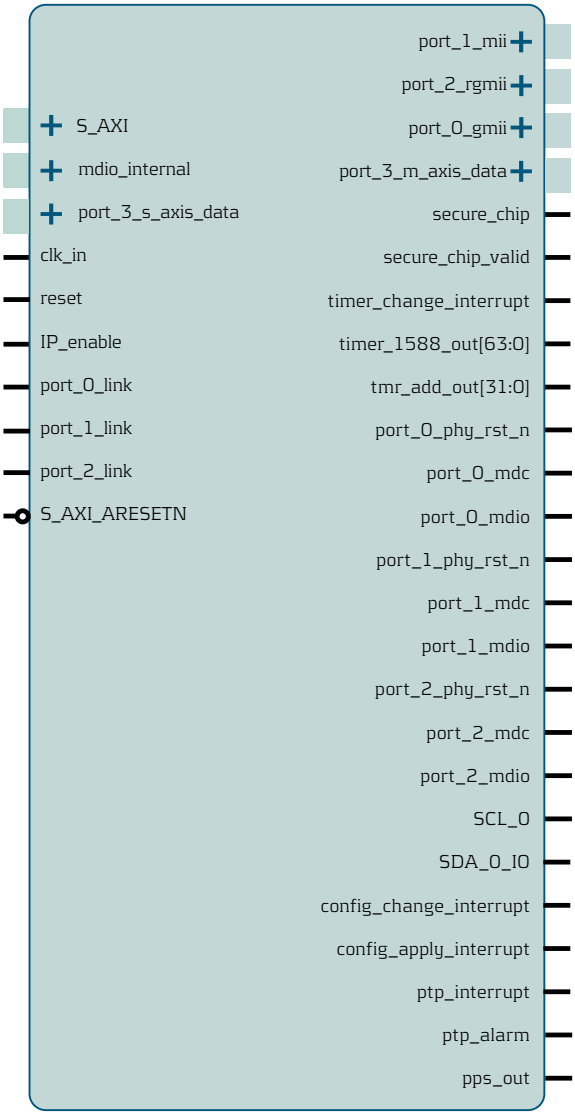
Configuration

- MDIO, UART, AXI4-lite or Configuration-over-Ethernet (CoE) management interfaces

Support

- RESTCONF/NETCONF YANG model support (CNC configuration)
- High-level Configuration GUI
- Drivers and software middleware provided
- Reference Designs and Evaluation Kits available: MTSN Kit

10G Multiport TSN Switch



Multiport TSN Switch

The demand for higher data-bandwidth of TSN-based backbones is increasing. The aggregation of OT traffic combined with IT one in the Smart Factories, Radar and Lidar sensor fusion in Automotive and 5G nodes are good examples of the demand that pushes this evolution. SoC-e **10G Multiport TSN Switch** benefits from the Generation 4 switching matrix developed by SoC-e. This matrix is already applied in the10G Managed Ethernet Switch IP core. In addition to the general features detailed for that IP, 10G Multiport TSN Switch includes means to support TSN capabilities.

TSN Profiles

A relevant indicator the level of interest on new protocols and networking technologies is the number and the maturity level of Profiles promoted by each Sector for a given standard. Industry is pushing IEC/IEEE 60802 TSN Profile for Industrial Automation. This profile agrees the mandatory and the optional technical features that all TSN equipment should comply in order to interoperate in the factory of the future. Other sectors like Automotive -P802.1DG – TSN Profile for Automotive In-Vehicle Ethernet Communications-, 5G and Telecom -P802.1DF – TSN Profile for Service Provider Networks- or Aerospace -AS6675 Aerospace TSN Profile- are working in the specifications.

1G HSR/PRP Switch

SoC-e HSR/PRP Switch IPs implement bumpless Ethernet connectivity ensuring zero-delay recovery time in case of network failure and no-frame lost. These IPs support the latest version of High-availability Seamless Redundancy (HSR) and Parallel Redundancy Protocol (PRP) standards in combination with redundant IEEE 1588-2008 for sub-microsecond synchronization. The flexibility and scalability of this IP offer optimized solutions for cost-sensitive CPU-less equipment and for high-end SoC based networking platforms.

Each HSR/PRP port pair is implemented with a dedicated hardware module in order to ensure the best performance of the switching operations. These modules can be easily combined with other SoC-e Ethernet IPs to implement heterogeneous switches that mix standard, high-availability and deterministic Ethernet ports.

Key Features:

Interfaces

- Full-duplex 10/100/1000 Mbps Ethernet Interfaces
- MII/RMII/GMII/RGMII/SGMII/QSGMII Physical Layer device (PHY) interfaces
- Copper and Fiber-optic media interfaces: 10/100/1000Base-T, 100Base-FX, 1000Base-X

Switching

- IEC 62439-3 (clauses 4-5) v3
- Optimized architecture to avoid HOL effect
- Cut-through and Store & Forward combined switching architecture
- CPU-less version available
- Distributed memory architecture for maximum reliability and scalability
- Traffic segregation based on Ethernet Type with dedicated memory buffers support
- QoS based on PCP-802.1p
  Timing
- IEEE 1588v2 P2P Stateless Transparent Clock operation processed by hardware

Security

- IEEE 802.1X and EAPOL hardware support
- Supervision Frames managed by hardware

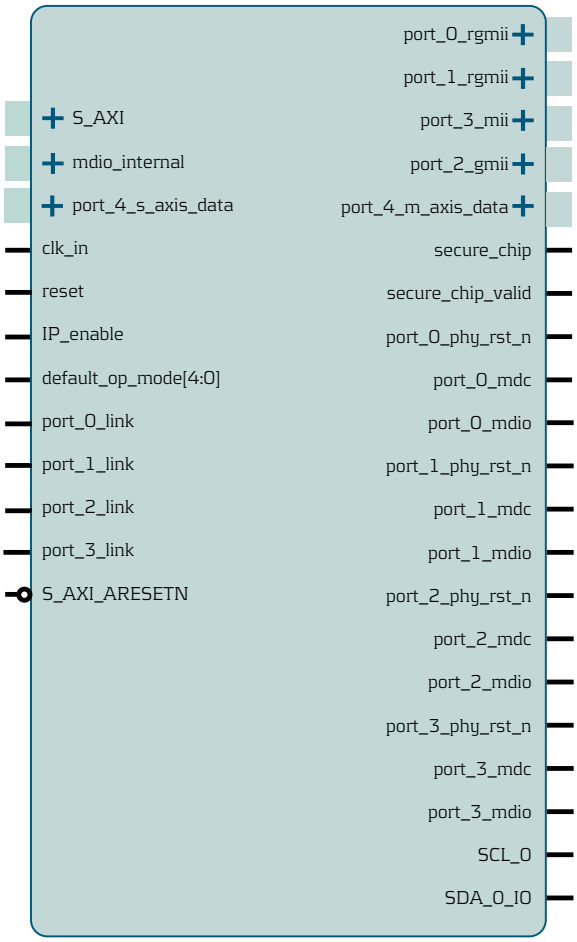
Configuration

- MDIO, UART, AXI4-lite or Configuration-over-Ethernet (CoE) management interfaces

Support

- Xilinx Spartan-6/Virtex-6, 7-Series and Ultrascale/Ultrascale+ devices and newer FPGA/SoC devices supported
- Reference Designs and Kits available (SMARToem, SMARTmpsoc, SMARTzynq, MEZU)

D-S HSR Switch



Managed Redundant Switch

In addition to standard HSR/PRP, SoC-e offers support for **Deterministic HSR (D-HSR)**. It is a hardware based solution for applications where the timing and bandwidth use restrictions are severe. In these cases, it is necessary adding a timing plane to the HSR nodes in order to deliver the data traffic in a scheduled way. IEEE 1588 protocol is the driver to build a deterministic HSR solution focused on rugged sectors like Electric or Defense that prefer a robust hardware-based solution simpler than the general purpose TSN one.

If cybersecurity is a key requirement and data authenticity needs to be ensured, SoC-e offers **Secure HSR (S-HSR)**. This solution comprises a low-latency cryptographic implementation that allows simultaneous encryption and authentication. S-HSR frame format has been designed in order to ensure interoperability with standard HSR nodes. This feature facilitates the introduction of secure HSR equipment gradually.

10G Managed Ethernet Switch

10G Managed Ethernet Switch (MES) IP core features a full-speed, Head-Of-Line effect free crossbar matrix that allows continuous transfers between all the ports. It supports up-to 32 ports with different line speeds. The internal micro-architecture includes disruptive enhancements in order to ensure a reliable operation of the switch even in critical use-cases. As an example, Virtual Output Queues combined with mirrored MAC tables allow simultaneous access to the matrix at maximum data throughput. The IP does not require any external memory.

Key Features:

Switching

- Non-blocking full speed 10G switching matrix
- HOL-effect free
- Dynamic MAC Table with automatic MAC addresses learning and aging
- Static MAC Table
- Jumbo Frame Management
- Ethertype Based Switching
- Broadcast/Multicast Storm Protection

Interfaces

- Full-duplex 100M/1G/2.5G/5G/10G Ethernet Interfaces
- Configurable from 3 up-to 32 Ethernet ports
- MII/RMII/GMII/RGMII/SGMII/QSGMII/USXGMII Physical Layer device (PHY) interfaces
- Different data rate supported for each port
- Copper and Fiber optic media interfaces: 100M/1G/2.5G/5GBase-T, 100MBase-FX, 1GBase-X, 10GBase-SR, 10GBase-LR, 10GBase-BX

Time Synchronization

- IEEE 1588v2 Stateless Transparent Clock functionality (P2P - Layer 2/ E2E - Layer 2)

Traffic Management

- Multicast Frames Filtering
- Switching Portmask: User-defined forwarding of frames to concrete ports
- Port-based VLAN support
- Priorities (PCP-802.1p, DSCP TOS, Ethertype)
- DSA (Distributed Switching Architecture) tagging
- IGMPv2 snooping

Security

- IEEE 802.1X EAPOL hardware processing
- Per-Port Rate limiting (Broadcast, Multicast and Unicast traffic)
- Port Mirroring

Configuration

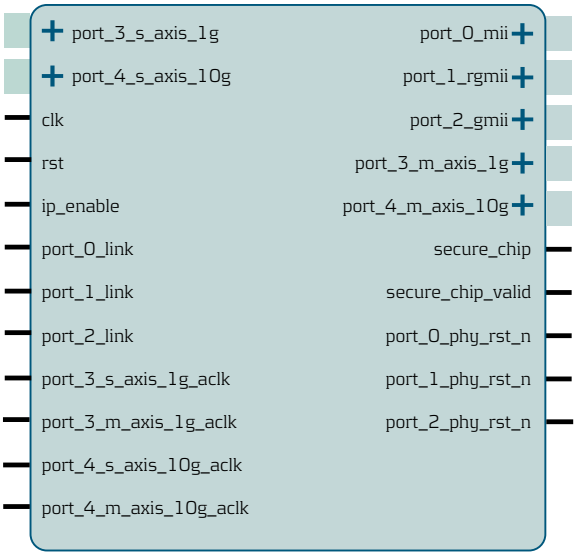
- MDIO, UART, AXI4-Lite or CoE (Configuration-over-ethernet) management interfaces

Redundancy

- M/RSTP (Software stack required)
- Hardware support for M/RSTP
- Reference M/RSTP stack for Linux provided with the IP Core
- Posix Compatible RSTP stack available

Support

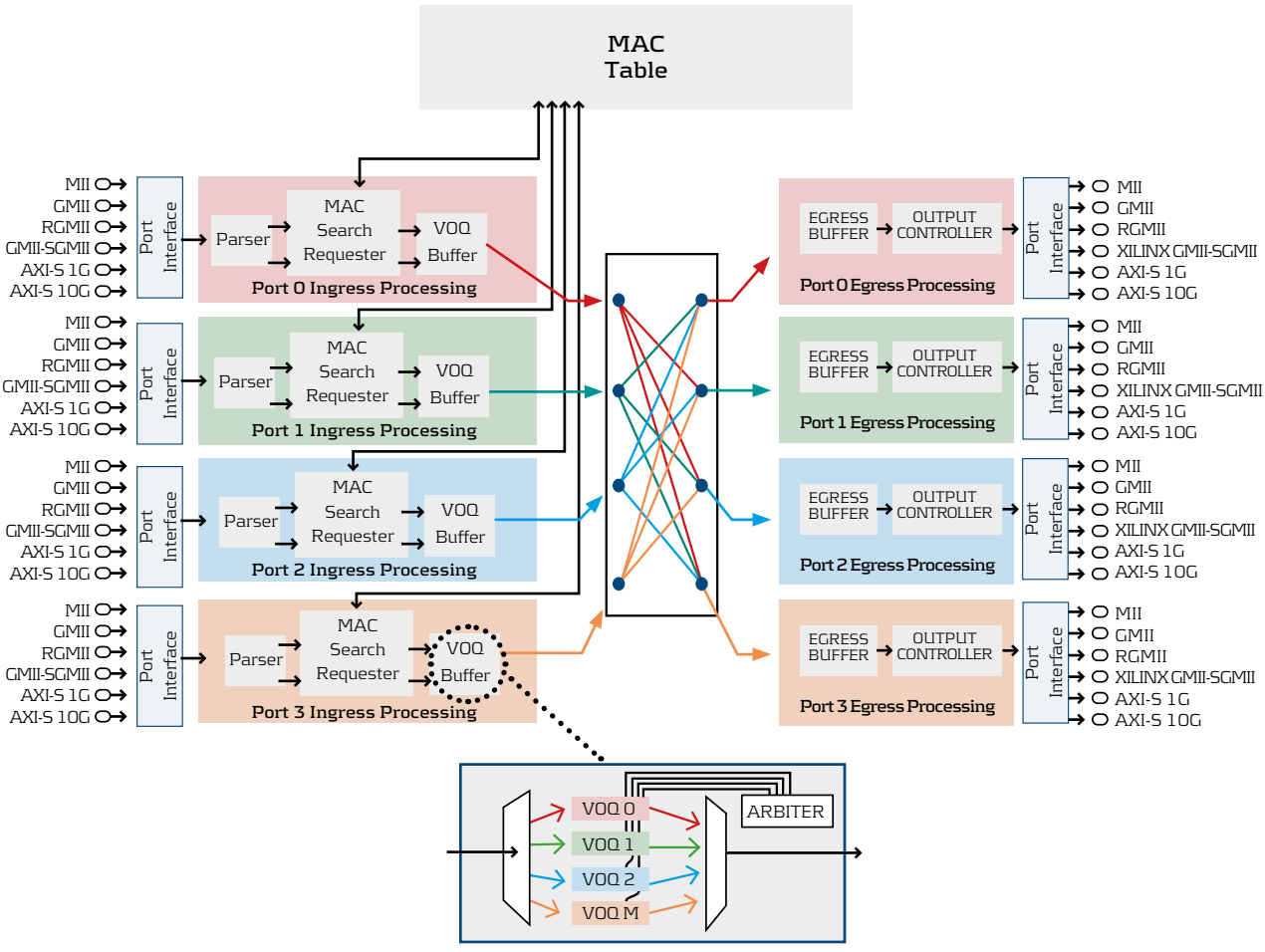
- Xilinx 7-Series and Ultrascale/ Ultrascale+ and newer FPGA/SoC devices supported
- Reference Designs and kits available



10G Managed Ethernet Switch

Head-of-Line effect in Critical Systems

One example of the impact of Head-of-Line (HOL) blocking is the degradation on real-time video streaming applications. Channel failures with non-HOL blocking free switches may reach some hundred milliseconds, making packets staying in the same queue and destined for other destinations be blocked and experience large delays. Additionally, in Critical Systems with hard real-time requirements for control communications, this misbehavior may be fully unacceptable.



1G Managed Ethernet Switch

The integration of Ethernet Switches on FPGA simplifies the communication between heterogeneous systems and applications. Thanks to the flexibility of reconfigurable devices combined with networking IPs, the end-equipment embeds not only Ethernet endpoint capabilities but added-value switching features as well. The low switching latency of SoC-e IPs implemented over a non-blocking matrix infrastructure is an added-value for networking in critical systems. Additionally, the IEEE 1588-2008 synchronization, the packet inspection for security or the storm protection mechanisms are fully implemented in hardware. This flexible architecture ensures the port number scalability and it simplifies the integration of these IPs in the systems.

SoC-e has developed a portfolio of Ethernet Switching IPs focused on different applications and sectors. Therefore, it is feasible combining the features of different IPs to obtain finally an optimal solution for each case.

The **1G Managed Ethernet Switch (MES) IP** is a powefull and flexible solution to integrate Ethernet support in any design.

Key Features:

Interfaces

- Full-duplex 10/100/1000 Mbps Ethernet Interfaces
- Half-duplex 10/100 Mbps Ethernet Interfaces
- MII/RMII/GMII/RGMII/SGMII/QSGMII Physical Layer device (PHY) interfaces
- Copper and Fiber-optic media interfaces: 10/100/1000Base-T, 100Base-FX, 1000Base-X
- 10 Gbps Ethernet Interface support (up to 10Gbps support in the uplink interface.)

Switching

- Non-blocking matrix architecture: 100% data throughput for GbE traffic
- From 3 up to 32 ports
- Optimized architecture to avoid HOL effect
- Fast frame forwarding (cut-through) support between predefined port pairs.
- Jumbo Frame support
- Quality of Service according the PCP bits (802.1p), the DSCP TOS bits of the IP packet or Ethertype

Timing

- IEEE 1588-2008 P2P/E2E Transparent Clock operation run by hardware
- IEEE 1588v2 Stateless Transparent Clock functionality (P2P/ E2E)
- Traffic Management
- Shared Dynamic and Static MAC Table (configurable size)
- Independent VLAN Learning support
- Multicast Frames Filtering
- Switching Portmask: User-defined forwarding of frames to concrete ports
- Port-based VLAN switching
- EtherType Based switching
- Priorities (PCP-802.1p, DSCP TOS, Ethertype)
- DSA (Distributed Switching Architecture) tagging
- IGMPv2 snooping
- Link Aggregation support

Security

- Security IEEE 802.1X and EAPOL hardware support
- Per-Port Rate limiting (Broadcast, Multicast and Unicast traffic)
- Port Mirroring: Ingress and/or egress traffic to any port

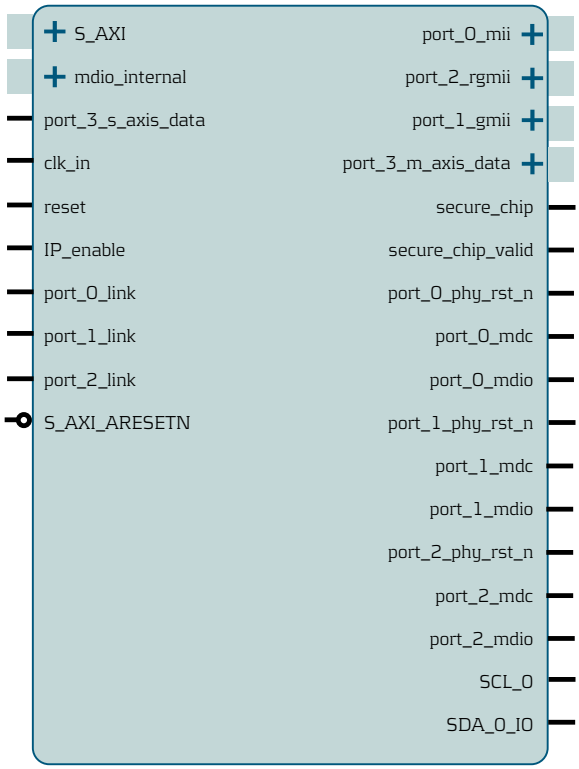
Redundancy

- Hardware support for M/RSTP
- Media Redundancy Protocol (MRP) support
- Device Level Ring (DLR) support
- Configuration
- MDIO, UART, AXI4-lite or Configuration-over-Ethernet (CoE) management interfaces

Support

- Xilinx Spartan-6/Virtex-6, 7-Series and Ultrascale/ Ultrascale+ and newer FPGA/SoC devices supported
- Reference Designs and kits available (SMARTmpsoc, SMARTzynq, MEZU)

Ethernet Networking



Managed Ethernet Switch

SoC-e Ethernet switch IP family includes an unmanaged version, named **Unmanaged Ethernet Switch IP**, that provides Plug&Work switch operation and it is optimized for an implementation that provides the maximum performance with minimal FPGA resources.

In combination with a Profinet software stack, **Profinet IP** is a tailored option providing support for Profinet RT CC-B Line Structure over multiple port.

Profinet and other field-buses relie on **Media Redundancy Protocol (MRP)** to ensure high-availability. This data network protocol has been standardized by the International Electrotechnical Commission (IEC) as IEC 62439-2 and it allows rings of Ethernet switches to overcome any single failure with recovery time much faster than achievable with traditional alternatives like Spanning Tree Protocol. MRP is optionally supported. Specifically, the roles of client (Media Redundancy Client – MRC) and manager (Media Redundancy Manager – MRM) are fully implemented on hardware in the IP, and there is no need for MRP software stack.

The support for legacy Field-buses is completed with the option for **Ethernet IP/DLR IP**. This multiport implementation supports DLR redundancy operation. The DLR management is done by hardware on port pair bases. The Beacon Based Node and Supervision operations are supported by hardware as well and they do not require an auxiliary CPU.

SoCe MES IP is a multi-sector product. As an example, it is embedded in the equipment for automation and protection for the Electric Grid. It is used to support Ethernet field-buses in Industrial PLCs and Networking equipment. Customers from the Automotive sector combines SoC-e MES and PTP IPs cores for LIDAR and Gateway applications. And Aerospace sector, benefits from MES IP low-latency and distributed memory architecture.

SpaceWire

Spacewire IP is a VHDL core that implements a complete, reliable and fast SpaceWire encoder-decoder with AXI management interface, synthesizable for FPGA and for reconfigurable SoC devices. SpaceWire protocol is a standard for high-speed links and networks for use on-board spacecraft, easing the interconnection of sensors, mass-memories, processing units and downlink telemetry sub-systems. It is a full-duplex, bidirectional, serial, point-to-point data link. It is applicable to many aerospace microelectronics devices like Spacecraft systems, Bus systems and Embedded microcontrollers. The evolution of this standard for Spacecraft communication networks is coordinated by the European Space Agency (ESA) in collaboration with international space agencies including NASA, JAXA, and RKA.

Data interfaces

- Reception Bit-rate up to x4 of the system clock frequency
- Transmission Clock Frequency between 100MHz-625MHz
- Separate Clock Domains

FIFO Configuration

- Transmission FIFO Depth fully configurable: From 64 bytes to 16384 bytes
- Reception FIFO Depth fully configurable: From 64 bytes to 16384 bytes

Interfaces

- AXI-Stream (Data)
- AXI-4 Lite (Configuration & Management)

Performance

- Up to 200Mbps Link Speed

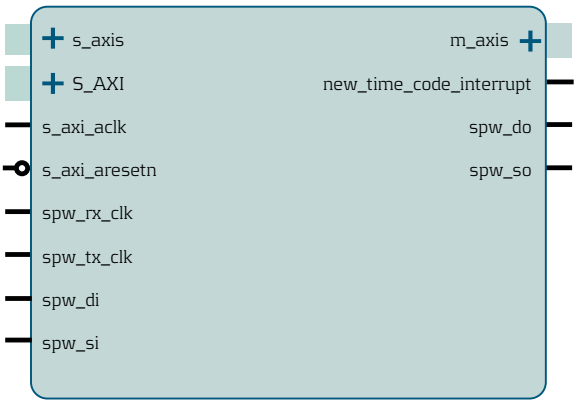
SpaceWire IP is used at the International Space Station in a custom Multi-core Reconfigurable SoC-based hardware developed by SoC-e for an Aerospace customer.

Cameralink RX Interface

Cameralink RX Interface is an HDL IP to interface with video devices provided with Channel Link® technology. Channel Link uses LVDS technology for transmitting digital data using a parallel-to-serial transmitter and a serial-to parallel-receiver to transmit data at rates up to 2.38 Gbps. The base Channel Link standard uses 28 bits to represent up to 24 bits of pixel data and 3 bits for Video Sync signals. Cameralink RX Interface accepts the four LVDS data streams and one LVDS clock, and then deserializes the data into 28 bits of parallel data and a clock and interfaces the data using the standardized on-chip bus used in the platform.

Key Features:

- Base mode supported
- Camera Link input interface
- Configurable parameters:
  - Cameral Link working Frequency
  - Number of pixels per line
- Tested with Hyperspec MV and e2v OCTOPLUS camera devices

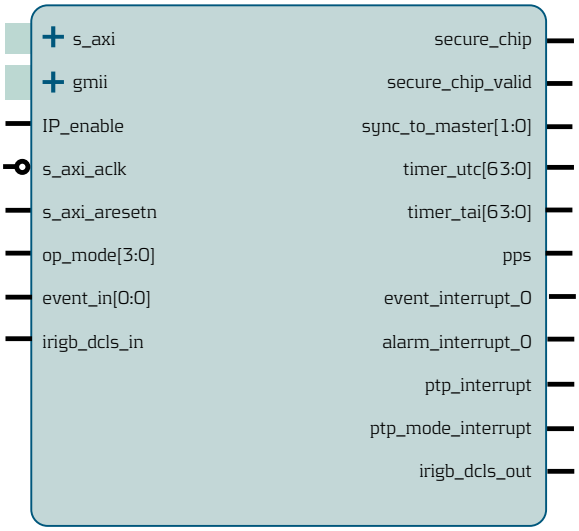


SpaceWire

MULTIsync

MULTIsync IP is a multi-protocol redundant time synchronization core that provides sub-microsecond time synchronization offering the maximum flexibility for every scenario. It can achieve accurate time synchronization using IEEE 1588-2006 (PTPv2) and IRIG-B time protocols. This versatility enables different use cases that are complementary:

- **Clocking source redundancy**: It is feasible connecting the IP to a PTP network and to an IRIG-B master at the same time. The user selects which is the time source used between the three available (PTP, IRIG-B, free running timer)
- **Clocking Bridge:** It runs as a PTP to IRIG-B or IRIG-B to PTP bridge while the IP is synchronized with the selected master
- **Clock Master Functionality:** It can act as PTP or IRIG-B master



MULTIsync

Key Features

- IRIG 200-04 compliant time synchronization master and slave
- Support for DCLS and AM modulations
- Support for all IRIG-B coded expressions, including year information, control functions and straight binary seconds
- Output type (IRIG-B timecode) configurable both before implementation and on-the-fly
- IEEE 1588v2 Profiles supported:
  - Default
  - Power
  - Power-Utility (IEC61850-90-3)
  - 802.1AS
  - Enterprise/5G/telecom: G.8265.1, G.8275.1, and G.8275.2
- Upgradeable to IEEE1588v2.1/v3 and to 802.1ASrev
- Synchronization input (slave) sources:
  - PTP: Ethernet. PTP Slave at the input
  - IRIG-B: IRIG-B compliant signal. IRIG-B Slave at the input
- Free Running Timer: Digital input
- Synchronization output (master) options:
  - PTP: Ethernet. PTP master at the output
  - IRIG-B: IRIG-B compliant signal. IRIG-B master at the output
  - Free Running Timer: Digital Output
- Xilinx Spartan-6/Virtex-6, 7-Series and Ultrascale/ Ultrascale+ and newer FPGA/SoC devices supported

CLOCK MULTI-SOURCE

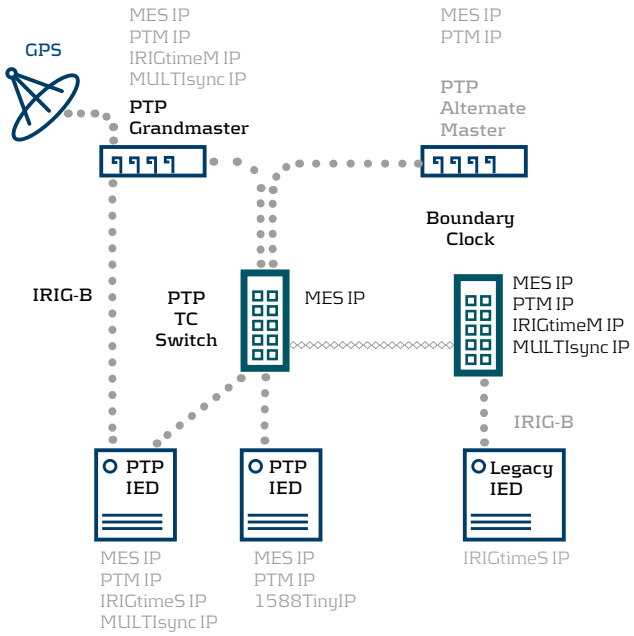
The evolution of timing and synchronization distribution mechanisms over the last decades has opened an opportunity for Timing Gateway equipment. Equipment capable of working as Master and Slave combining IRIGb, NTP, PTP and GPS/GNSS sources offer a valuable solution for Electric and Aerospace & Defense sectors that demand bridging from different technologies. These synchronization IPs from SoC-e are in the heart of many of this flexible equipment.

Accurate Timing Synchronization

IEEE 1588-2008 Precise Time Multi-Profile

Precise Time Multi-Profile IP provides an outstanding synchronization mechanism that only requires Ethernet connection to obtain nanosecond range synchronized timers in the equipment. Precise Time Multi-Profile is capable of accurately timestamping IEEE 1588 telegrams. The IP embeds timers, registers, interfaces and auxiliary signals to provide the additional features described below. The IP is delivered with all the necessary software to run in combination with an internal or external CPU.

Precise Time Basic



Key Features:

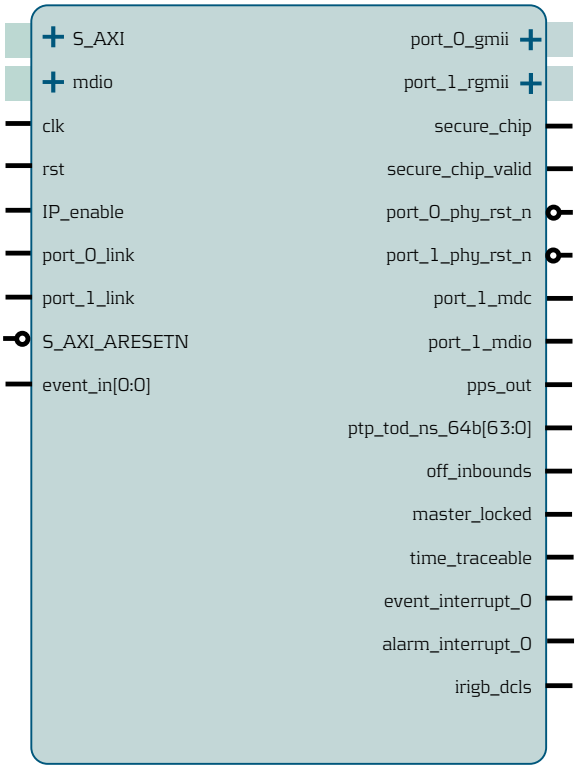
- Hardware and software to support Gran Master, Ordinary, Transparent and Boundary Clock functionalities
- GMII or AXI-4 Stream selectable interfaces to support:
  - » Full-duplex 10/100/1000 Mbps Ethernet
  - » Half-duplex 10/100 Mbps Ethernet
  - » Full-duplex 10 Gbps Ethernet
  - » Full-duplex 25 Gbps Ethernet
- 32 bit seconds / 32 bit nanoseconds counter
- 32 bit sub-nanosecond frequency adjust
- Pulse Per Second (PPS) Output available
- Frequency Selectable Output available (1 KHz/2 KHz/4 KHz/8 KHz/16 KHz/32 KHz)
- External event timestamping logic
- Programmable alarms defined by the user
- PTP on both Layer 2 (Ethernet) and Layer 3 (IPv4) interfaces supported
- Seamless integration with HSR-PRP and Ethernet IP Switch cores
- VLAN support
- IEEE 1588v2 Profiles supported:
  - » Default
  - » Power
  - » Power-Utility (IEC61850-90-3)
  - » 802.1AS
  - » Enterprise/5G/telecom : G.8265.1, G.8275.1, and G.8275.2
- Upgradeable to IEEE1588v2.1/v3 and to 802.1ASrev
- Xilinx Spartan-6/Virtex-6, 7-Series and Ultrascale/ Ultrascale+ and newer FPGA/SoC devices supported
- Specific version for Xilinx Ethernet subsystems (10G/25G and above)

PTP Profiles

Precise-Time-Protocol (PTPv2), released as IEEE 1588-2002 standard, is providing GPS-range timing synchronization through the networking infrastructure to Finance, Wireless, Aerospace, Military, Industry & Smart Grid. The adoption of specific PTP profiles by each sector shows the relevance of this protocol in the modern systems. As an example, the Electric sector has adopted the fail-safe IEC/IEEE 61850-9-3 Power-Utility profile. The Telecom is evolving fast their Enterprise/5G/Telecom profiles (G.8265.1, G.8275.1, and G.8275.2) to fulfill the requirements of 5G transportation networks. And Automotive, has focused on IEEE 802.1AS to support advanced QoS for audio and video broadcasting.

1588Tiny Slave-Only

1588Tiny IP offers the simplest solution available in the market to integrate IEEE 1588-2008 slave clock capabilities to any equipment. 1588Tiny embeds the Ethernet MAC, parsing and timestamping units and the computation logic required to output a synchronized clock and a PPS output. This IEEE1588v2 Slave Only compliant clock synchronization IP core is focused on equipment that requires basic IEEE 1588 functionality using the minimum resources and complexity. Therefore, 1588Tiny does not need any software and it can run in CPU-less boards. This IP can be combined with HSR-PRP and Ethernet Switch IPs to implement stand-alone Hybrid Clocks with switching capabilities.



1588Tiny

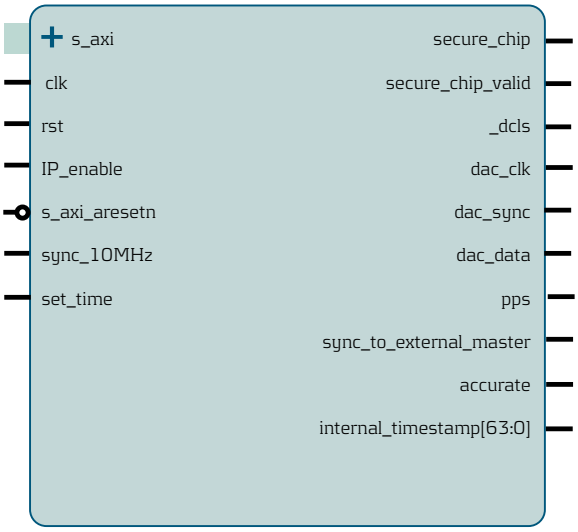
Key Features:

- CPU-less operation (no software required)
- IEEE 1588v2 slave -only operation
- 64 bit Timer value available to customer logic
- Embedded Ethernet interfaces to support:
  - Full-duplex 10/100/1000 Mbps
  - Half-duplex 10/100 Mbps
- Full-duplex 10 Gbps support through AXI-4 Interface
- PPS output signal
- Optional IRIG-B Master Output
- IEEE 1588v2 Profiles supported:
  - Default
  - Power
  - Power-Utility (IEC61850-90-3)
  - 802.1AS
- Upgradeable to IEEE1588v2.1/v3 and to 802.1ASrev
- Xilinx Spartan-6/Virtex-6, 7-Series and Ultrascale/ Ultrascale+ and newer FPGA/SoC devices supported

Accurate Timing Synchronization

IRIG-B Master

This IP implements an IRIG 200-04 compliant time synchronization master on FPGA devices. It has been designed to support all the IRIG-B coded expressions as well as DCLS and AM modulations providing the maximum flexibility and accuracy.



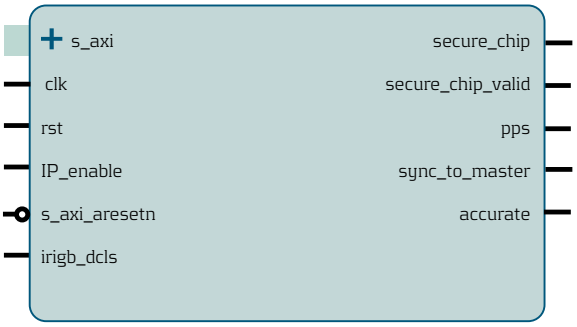
IRIGtimeM

Key Features:

- IRIG 200-04 compliant time synchronization master
- Support for DCLS and AM modulations
- Support for all IRIG-B coded expressions, including year information, control functions and straight binary seconds
- Output type (IRIG-B timecode) configurable both before implementation and on-the-fly
- Precise IRIG-B output in order to provide nanosecond range precision
- 32-bit timestamp input for initial set up of the IP
- Periodic pulse output for testing
- Autonomous operation by hardware

IRIG-B Slave

This IP implements an IRIG 200-04 compliant time synchronization slave on FPGA devices. It has been designed to support all the IRIG-B coded expressions as well as DCLS and AM modulations to provide maximum flexibility, accuracy and autonomy.



IRIGtimeS

Key Features:

- IRIG 200-04 compliant time synchronization slave
- Support for DCLS and AM modulations
- Support for all IRIG-B coded expressions, including year information, control functions and straight binary seconds
- Sub-microsecond synchronization with the IRIG-B master
- 64-bit internal timer synchronized in time and frequency with the IRIG-B master
- 32-bit for timestamp in seconds and 32-bit for nanosecond
- Periodic pulse output for testing
- Autonomous operation by hardware

Multi-algorithmic low-latency AES-GCM Crypto-core

This cryptographic IP core has been specifically designed to target a wide range of applications as it is able to protect and authenticate high data throughputs with a very low latency. The IP core is fully customizable, being possible to select the perfect trade-off between resource utilization and performance that suits each specific use case.

Key Features:

- Encryption, decryption and dual (both encryption and decryption) operation modes supported
- 128 bit key size supported
- Adjustable performance at synthesis time from 3 Gbps up to 16 Gbps
- Selectable Galois multiplication engine for improved resource usage or timing
- Separated AXI-4 Stream interfaces for each data type:
  - Key
  - Initialization Vector (IV)
  - Authenticated data
  - Plaintext
  - Ciphertext
  - Authentication TAG

Secure Configuration-over-Ethernet IP

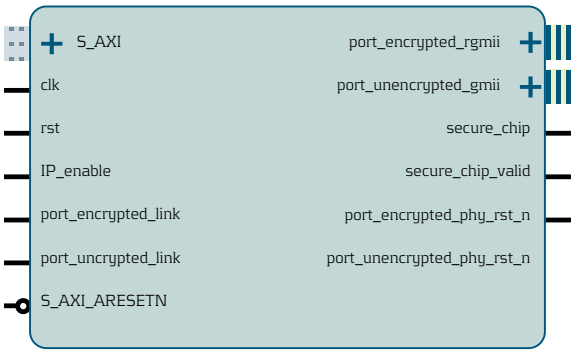
SoC-e offers a Layer-2 Ethernet based, configuration protocol to upgrade securely CPU-less FPGA systems. **Secure CoE** is useful to access the FPGA from off-board CPUs or SCADA/PC systems using Ethernet data link. This IP supports authenticated and encrypted CoE frames to enable the use of this protocol on public networks.

Key Features:

- Configuration and control protocol over Ethernet between external CPU or SCADA/PC and the FPGA
- AES-GCM secured
- Reduced FPGA resources utilization
- Software API and program examples provided for the CPU or PC system

Secure Ethernet for Substation Automation Systems Crypto-core

This IP faces the challenge of securing the most time-critical control messages in SAS and Smart-Grid: GOOSE and Sample Measured Values. The new generation of equipment for these specialized sectors needs to offer the highest level of reliability and security. Thanks to this IP, it is feasible implementing the most exigent security standards maintaining the mandatory tight reaction time defined in the IEC 61850 standard.



SASCrypt*

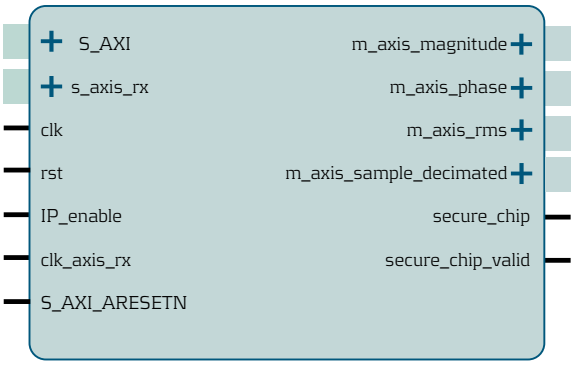
Key Features:

- GOOSE & SVM secured frame format support (IEC 62351-6, optional IEC 61850-90-5)
- Cipher and decipher operation
- Low-latency AES-GCM cipher suite embedded
- Wire-speed operation supporting up to 16 Gbps of continuous traffic
- Minimum latency time for tightly real time constrained GOOSE and SVM messages
- Designer selectable latency/throughput/FPGA resources trade-off
- Key management according to IEC 62351-9
- Combinable with SoC-e networking IPs

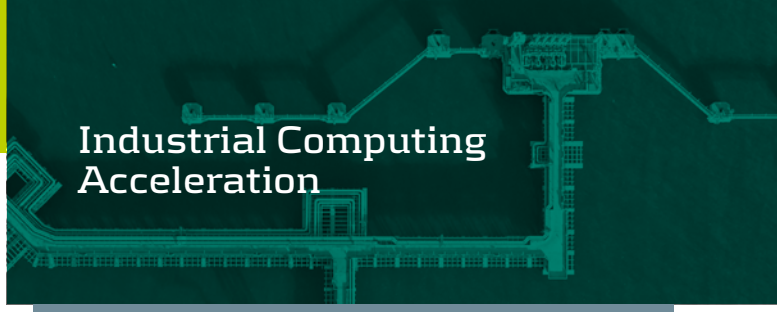
Sampled Measured Values Subscriber

SMVsubscriber IP analyses incoming traffic and detects IEC 61850-9-2 Sampled Measured Values (SMV) frames. According to several configuration parameters, selected SMV frames are processed, extracting the sampled values of current and voltage for the four phases (A, B, C and N). The IP uses those sampled values to perform the computation of the Discrete Fourier Transform (DFT) to get the angle and magnitude as well as the Root Mean Square (RMS) of each phase. It also provides the samples with the user defined decimation rate. The Sampled Measured Value (SMV or SV) Process Bus concept was introduced by the IEC 61850-9-2 standard. This standard proposes that the Current and Voltage Transformer (CT, VT) outputs and other signals are digitized at the source and then communicated to those devices using an Ethernet-Based Local Area Network (LAN).

This IP allows processing a massive number of SMV streams with a very low latency taking benefit from parallel hardware processing on FPGAs.



SMV Subscriber



Industrial Computing Acceleration

Deep-packet Inspection Engine

Key Features:

- Layer 2 IEC 61850-9-2 (SMV) frame processing
- High performance implementation of DFT computation module for calculating magnitude and phase of the first harmonic (50 or 60 Hz)
- High performance RMS computation module (up to 1562500 calculations/s)
- Up to 128 simultaneous SMV streams supported (up to 320 streams depending on the process Window configuration)
- Deterministic latency time for full computation of 6us
- Status, configuration and statistic counter registers
- 1000 Mbps AXI-Stream interface for seamless on-chip communications and combination with SoC-e networking IPs (HSR/PRP, Ethernet, TSN)
- Xilinx Alveo PCIe accelerator card supported
- Relyum RELY-SV-PCIe card supported

Sampled Measured Values

The original application for the SMVs was simplifying the cabling infrastructure and improving the availability at the Process Bus of the Power Substations. In this context, the grid protection mechanisms are managed based on the fault analysis of the current and voltage.

Once this digitalization mechanism has gained acceptance in the sector, new applications and use-cases are arising. As an example, the Industry has identified that the Fault Detection on Cable Sections in underground high-voltage lines can benefit from this digitalization. New use-cases are also arising in the field of Big Data like the use of SMV for Power Quality analysis done at Sundom Smart Grid (SSG) pilot. The emerging spread renewable energy sources identified as Distributed Energy Resources (DER) and Microgrids demand real-time response. This actuation needs to be evaluated in base of real-time measurements and high-speed networking.

As it can be observed, if this approach is scaled in several strategic locations of the Grid, the number of SMV streams that would need to be transmitted and processed increases drastically. This challenge can hardly be afforded by conventional IEDs due to their constrained networking and computation capabilities.

SoC-e provides an on-chip solution for tailored networking frames analysis and classification. **Deep-packet Inspection Engine (DIE) IP** supports wire-speed operation for high data bandwidth. The portfolio of available solutions covers security and IEC 61850 packet analysis applications among others.

Key Features:

- VHDL coded IPs
- Wire-speed operation for high data bandwidth links
- Full data pipelined hardware implementation
- AXI-4 Interfaces

FPGA Networking Module

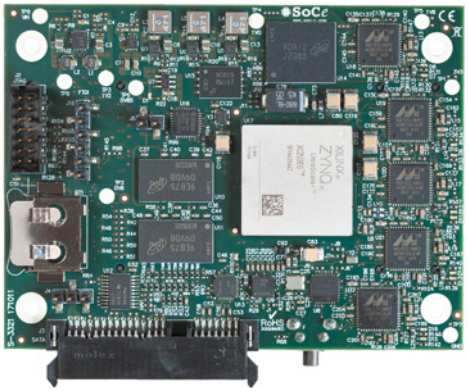
SMARTmpsoc is working as TSN capable Edge-Computing node for Video preprocessing in Factory Automation and Aerospace applications.

The new generation of reconfigurable System-on-Chip devices embeds heterogeneous CPU to offer the maximum flexibility and computing capabilities for Edge computing applications. SoC-e has designed **SMARTmpsoc**, a pluggable System-on-Module (SoM) to simplify the integration of custom networking and synchronization capabilities combined with these powerful Edge-computing capabilities.

The heart of this SoM is a long-term supply Xilinx Zynq MPSoC Ultrascale+ reconfigurable device that includes 6 ARM processors, a GPU and a high-end FPGA in a single device. The module is completed with industrial grade Gigabit Ethernet phys, SATA-3 connector for high-capacity data storage units, dedicated integrated circuit for security functions and RAM and Flash memory devices.

Applications:

- Edge computing device with advanced Ethernet networking capabilities
- TSN endpoint nodes and bridges
- Managed HSR/PRP/Ethernet embedded switch
- Synchronization device (Full IEEE 1588-2008 support)
- Network SoM for critical-mission applications
- Cybersecurity appliance: IDS, SIEM agents, on-the-fly encryption, etc.



SMARTmpsoc Module

Module:

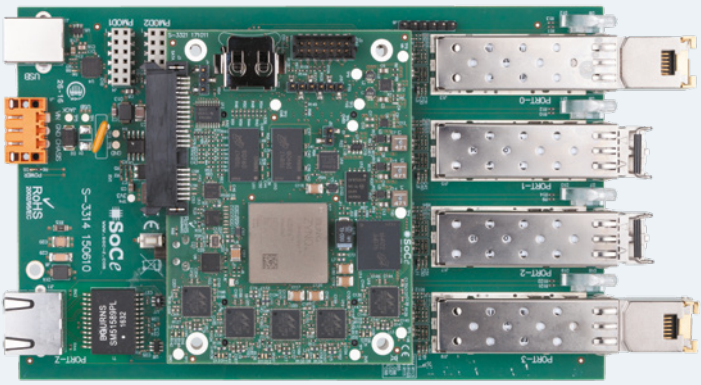
Key Features:

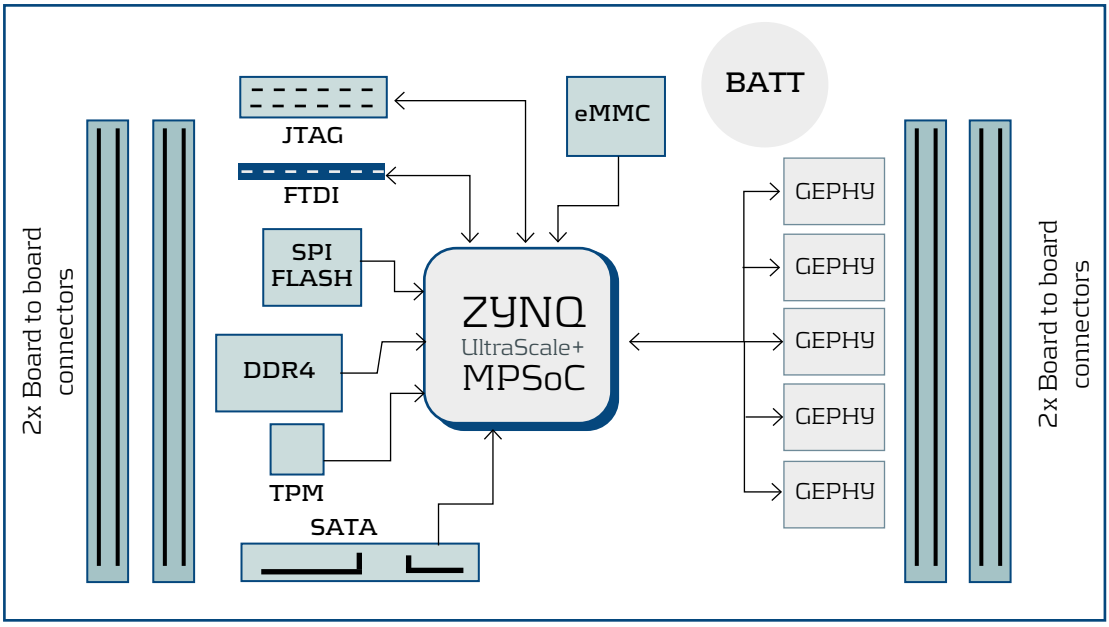
- Xilinx Zynq MPSoC Ultrascale+ XCZU3EG-SFVA625-1-I
- Optional XCZU2EG device
- Rugged for industrial applications
- Heterogeneous CPUs in a single IC:
  - 4x ARM Cortex-A53 CPUs
  - 2x Dual-core ARM Cortex-R5 CPUs,
  - 1x Mali™-400 MP2 GPU
  - High-end Ultrascale+ FPGA
- 5x Ethernet Phys 10/100/1000Base-T,-X
- 3x PS-GTR Transceivers
- 2 GB DDR4 RAM memory
- 32MB up to 64MB Quad SPI Flash Memory
- 16GB eMCC Flash memory
- Battery for Real Time Clock (RTC)
- Trusted Platform Module (TPM) 1.2/2.0 security Chip
- SATA-3 Connector
- Footprint compatible with SMARTzynq and SMARToem SoMs
- Size: 88x66 mm

SFP Brick:

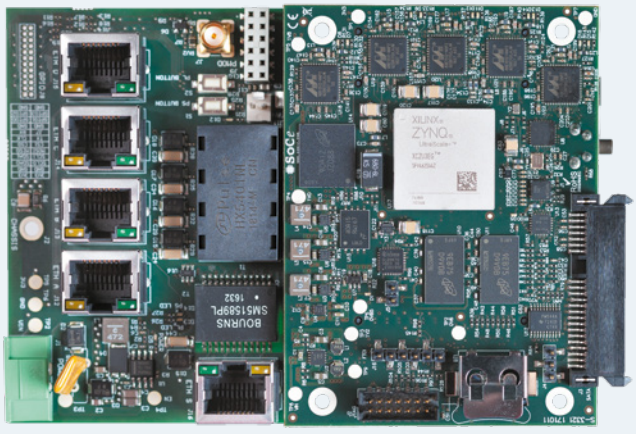
Key Features:

- 4x SFP cages for 10/100/1000Base-T, 100Base-FX or 1000Base-X
- 1x RJ45 for 10/100/1000BaseT
- UART console (USB)
- 6V-30V DC (Power supply included)
- 2x PMOD connectors





SMARTmpsoc



RJ45 Brick:

Key Features:

- 5x RJ45 for 10/100/1000Base-T
- UART console (USB)
- 6V-30VDC (Power supply included)
- 1x PMOD connector
- 2x Leds
- 2x Buttons
- 16x GPIO connector

Extended Brick:

Standard Brick Functionalities plus:

- USB Support
- Connection to 3x PS-GTR transceivers supporting:
  - » SGMII connectivity
  - » High-speed connectivity standards

Kits:

- 1588-aware HSR/PRP/Ethernet Switch Module
- MTSN Kit: a Comprehensive Multiport TSN Setup

FPGA Networking Module

SMARTzynq modules are used in many tailored applications that require software, time-aware networking and customer specific FPGA design. As an example, SMARTzynq configured with SoC-e IPs for high-availability networking is embedded on Power Automation and Protection equipment, in Railway signaling applications or in Intelligent Gateways for Industry 4.0.

The heart of the **SMARTzynq family** is a pluggable System-on-Module (SoM) designed to enable easy integration of specialized Gigabit Ethernet switches in smart equipment for Electric, Industrial and Aerospace sectors. The Zynq programmable SoC platform embedded in the board includes a high-end FPGA and a dual core ARM9 CPU able to drive 5x tri-speed Ethernet ports combining hardware IPs and software processing.

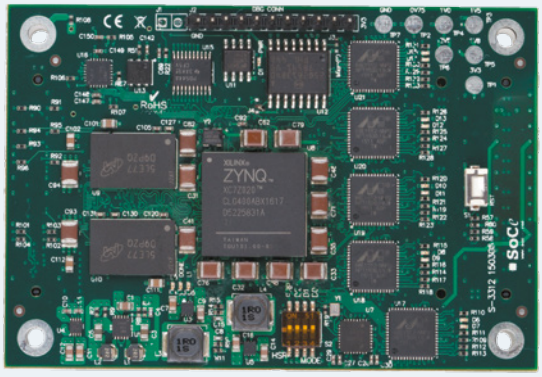
Applications:

- Managed HSR/PRP/TSN/Ethernet embedded switch
- IEEE 1588-2008 Master, Slave and Boundary Clock equipment
- Out-of-the-box embedded CPU solution
- TSN endpoint nodes and bridges
- Smart gateways for heterogeneous networks interconnection
- Advanced Cybersecurity applications: NDIS, SIEM agents, on-the-fly encryption, etc.

Module SMARTzynq:

Key Features:

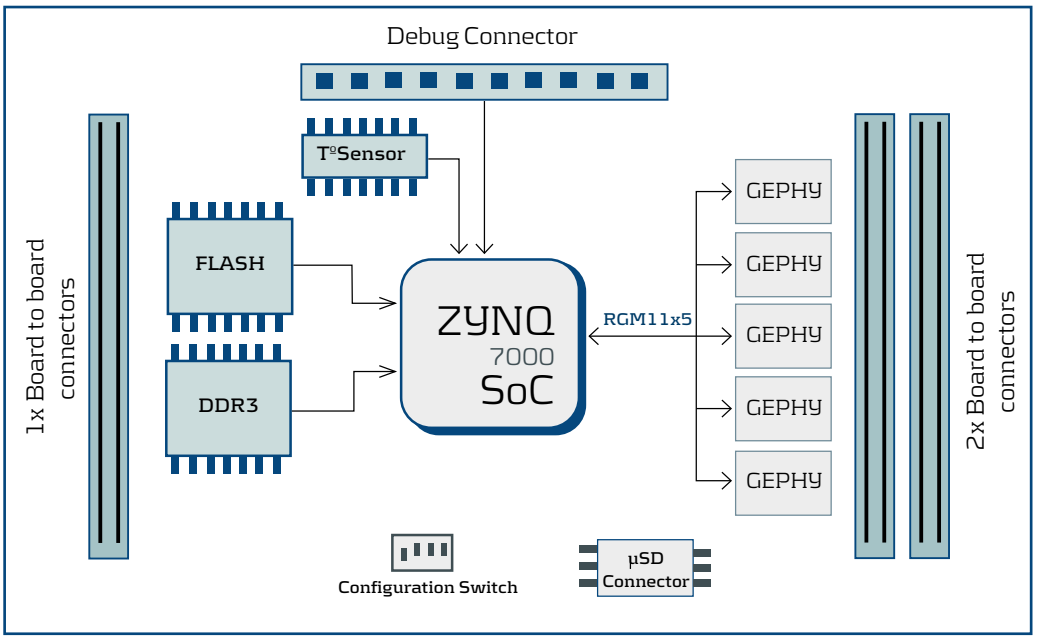
- Xilinx Zynq Programmable SoC XC7Z7010-7020
- Rugged for industrial applications
- Dual-core 32 bit ARM Cortex-A9
- 5x Ethernet Phys 10/100/1000BaseT-X
- 8 Gb DDR3 RAM memory
- 128Mb QSPI Flash memory
- EEPROM with unique MAC address
- Embedded Temperature Sensor
- uSD card memory
- Size: 88x60mm



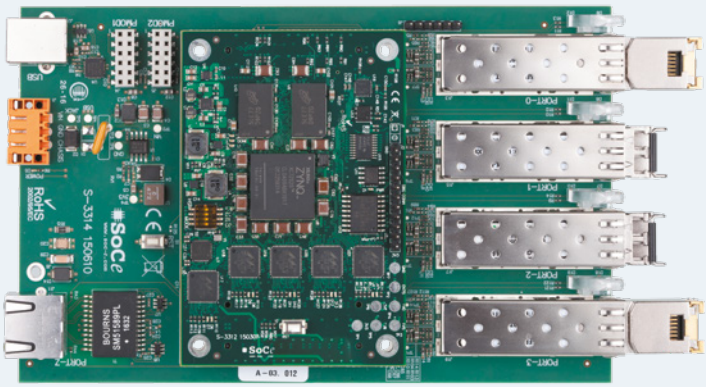
Module SMARTzynqIO:

Key Features:

- Xilinx Zynq Programmable SoC XC7Z7010-7020
- Rugged for industrial applications
- Dual-core 32 bit ARM Cortex-A9
- 4x Ethernet Phys 10/100/1000Base-T,-X
- 8 Gb DDR3 RAM memory
- 128Mb QSPI Flash memory
- EEPROM with unique MAC address
- Embedded Temperature Sensor
- 16GB eMCC Flash memory
- Up to 28x PL GPIOs
- Up to 22x PS GPIOs (USB 2.0 ready, SPI bus ready, UART ready)
- Size: 88x60mm



SMARTzynq



Brick:

Key Features:

- 4x SFP cages for 10/100/1000Base-T, 100Base-FX or 1000Base-X
- 1x RJ45 for 10/100/1000Base-T
- UART console (USB)
- 6V-30V DC (Power supply included)
- 2x PMOD connectors

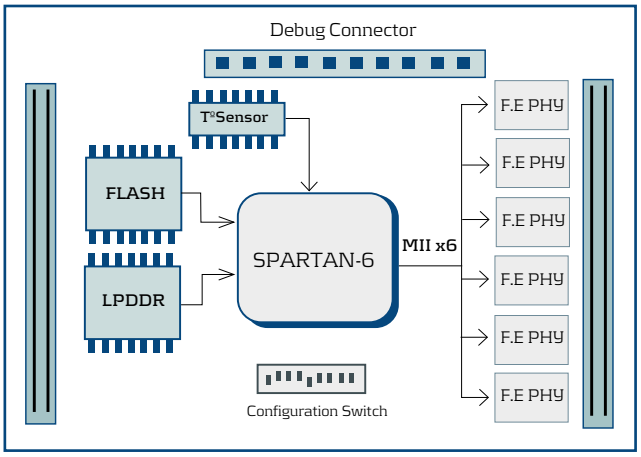
Kits:

- 1588-aware HSR/PRP/Ethernet Switch Module
- MTSN Kit: a Comprehensive Multiport TSN Setup

FPGA Networking Module

SMARToem Family

SMARToem family enables easy integration of added-value Ethernet Networks in equipment for Electric, Industrial and Aerospace sectors. The heart of the system is a Spartan-6 Xilinx FPGA able to drive up to 6 Fast Ethernet ports. The module can be used to implement a user defined design or can be purchased with any of the SoC-e Networking and synchronization IPs. This module is field proven worldwide embedding IEEE 1588-aware HSR/PRP and Ethernet switching capabilities into end-equipment like IEDs, RTUs, military products and in distributed sensor infrastructures for traffic and transportation.



SMARToem

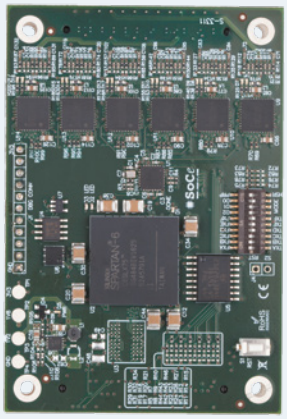
Applications:

- HSR/PRP/Ethernet embedded switch
- 1588-aware switches
- Hybrid Clock devices for distributed sensor acquisition
- Custom Ethernet switch
- Industrial Ethernet gateways
- Cybersecurity applications

Spartan-6 Module:

Key Features:

- Scalable Spartan-6 Xilinx FPGA LX45-LX150
- Rugged for industrial applications
- 6x Ethernet Phys 10/100Base-T, 100Base-FX+
- Support for Dynamic Bitstream Configuration (DBC)
- Support for Configuration-over-Ethernet (COE)
- Optional 512 Mb LPDDR
- 128 Mb Quad SPI Flash: Memory for Firmware and bitstream storage
- EEPROM with unique MAC address
- Embedded Temperature Sensor



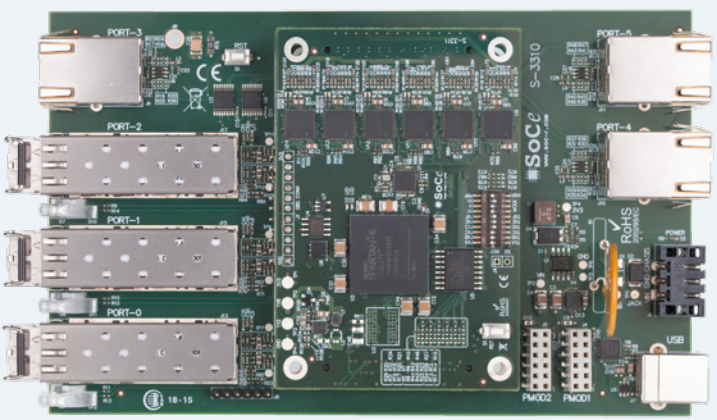
Spartan-6 Brick:

Key Features:

- SMARToem module
- Carrier for SMARToem module
- 3x SFP cages for 100Base-FX
- 3x RJ45 for 100Base-TX
- UART console (USB)
- 6V-30V DC (Power supply included)
- 2x PMOD connectors

Spartan-6 Kit:

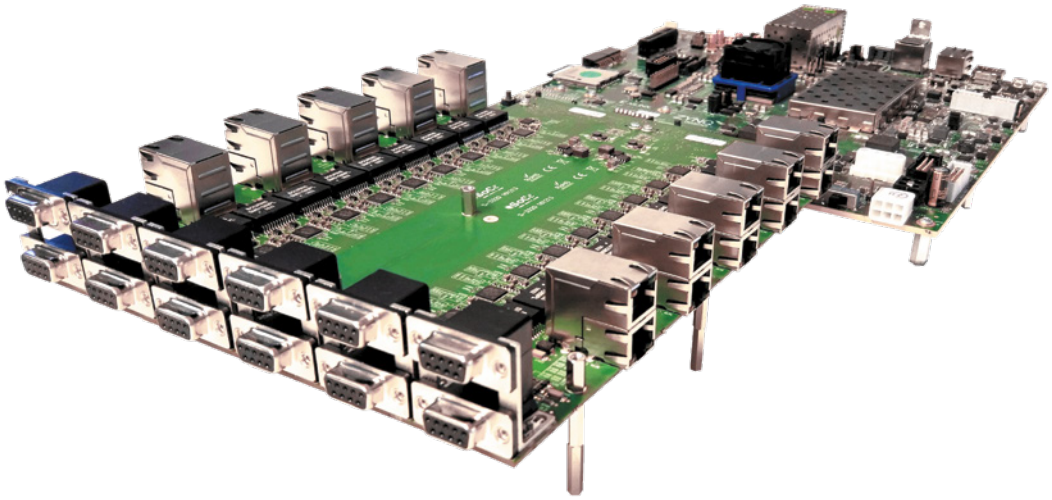
- 1588-aware HSR/PRP/Ethernet Switch Module

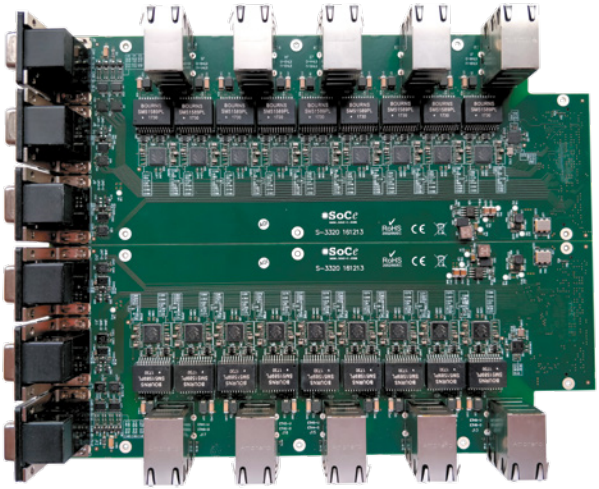


Multiport FMC Board

The Multiport FMC Board is a pluggable board that is compatible with most of FPGA vendors development boards that feature 1 or 2 FMC (HPC) ports.

It supports Ethernet, CAN-FD and LIN hardware connectivity. It is an excellent choice to implement FPGA based designs focusing the automotive sector.





Key Features:

- 18x 10/100/1000Base-T Ethernet Ports (16x use SGMII interface, 2x use RGMII interface) over RJ45 connectors
- 8x CAN-FD ports over DB9 connectors
- 8x LIN ports over DB9 connectors
- The board can be divided into 2x smaller FMC boards, each one using 1x FMC (HPC) port and featuring 9x 10/100/1000Base-T Ethernet , 4x CAN-FD and 4x LIN ports
- Industrial Temperature grade components

FPGA Networking Module

MEZU Family

MEZU family has been born taking into account the direct feedback received from our customers. It offers a cost-effective solution for flexible I/O combined with tailored time-aware Ethernet switching based on SoC-e IPs. The new MEZU devices integrate powerful computation capabilities to face new Machine Learning and AI applications over the OT/IT backbones.

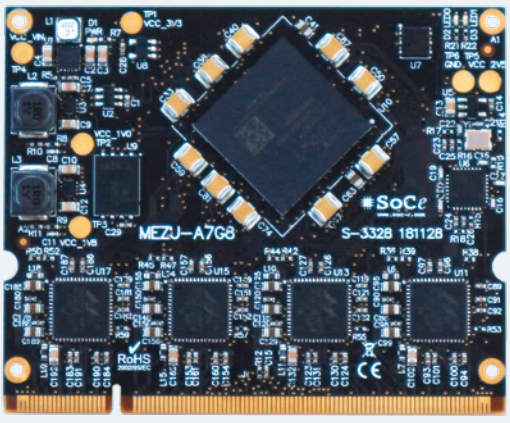
MEZU family is a pluggable SODIMM format set of modules designed to enable easy integration of Advanced Ethernet Industrial Networks in equipment for Electric, Transportation, Industrial and Aerospace & Defense sectors.

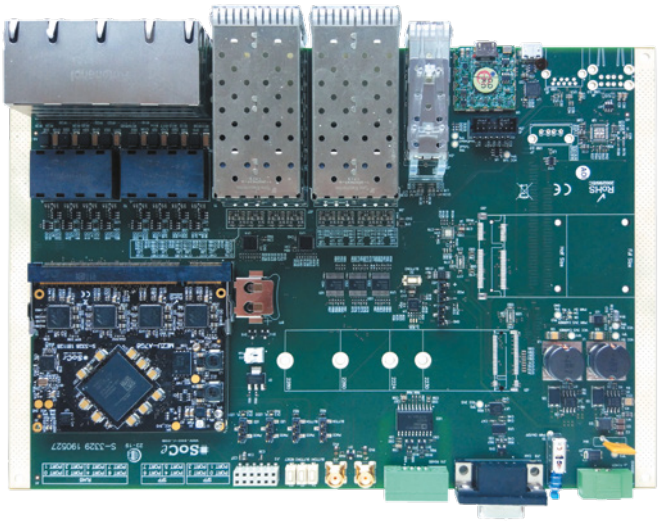
These cost-effective and easily integrable modules allow the implementation of custom routers, switches or end-equipment with powerful networking capabilities. The customer can use these modules to implement its own design or order them pre-loadedwith a configuration based on SoC-e IP cores.

A7G8 Module:

Key Features:

- 8x Ethernet Combo Phys
  - » Copper: 10/100/1000Base-T
  - » Fiber: 1000Base-X and 100Base-FX.
- Industrial Grade components
- Devices supported: Industrial Grade Xilinx Artix 7 XC7A50T, XC7A75T and XC7A100T
- 128/256/512 Mb Quad SPI Flash
- Size: 67.75 x 55 mm
- EEPROM with unique MAC
- 2x LEDs indicator.
- Up to 26 GPIOs ready to be used in the carrier
- SODIMM-DDR2 200 pin connector





MEZU Brick

Applications:

- IEEE 1588 Low-latency Ethernet Switching
- Zero-delay recovery time Ethernet (HSR/PRP)
- Other High-Availability Ethernet solutions: MRP, DLR-Ethernet IP, RSTP, etc.
- IEEE 1588 and IRIGb time synchronization solutions
- Wire-speed cryptography for Real-Time Traffic
- Time-Sensitive Networking
- Edge-Computing units
- SpaceWire for SpaceCraft standarized Networking

SOCG8 Module:

Key Features:

- New generation Xilinx reconfigurable Multi-core SoC
- 8x Ethernet ports
- Support for 100M/1G/2.5G/5G/10G Ethernet Interfaces
- SODIMM 200 pin connector
- Ready-to-use Linux based image
- Reference designs for 10GbE Ethernet and TSN

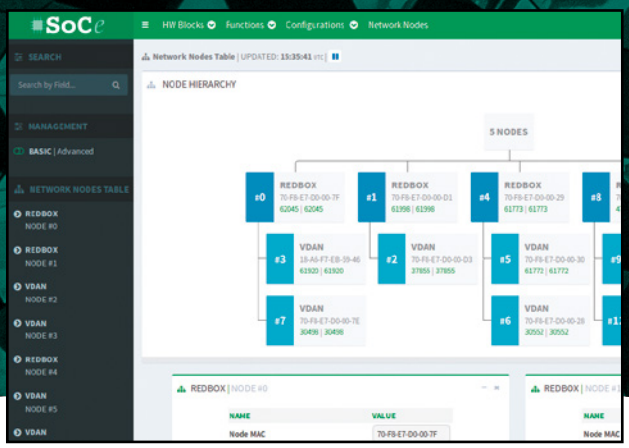
MEZU Brick:

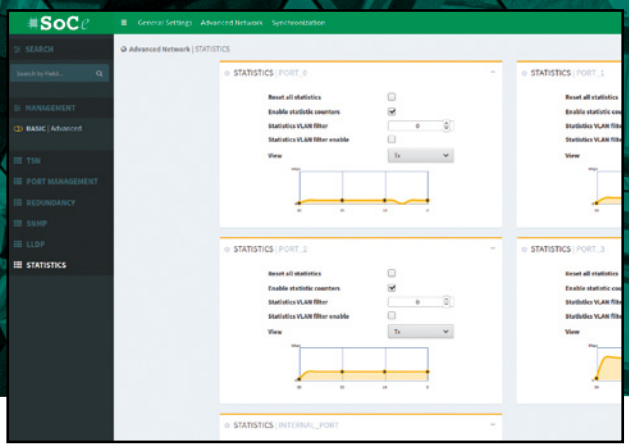
Key Features:

- Size: 6U (233 x 160 mm)
- 8x SFP cages
- 8x RJ-45 Gigabit Ethernet Connectors
- USB to UART bridge
- 2x Buttons (GP I/O)
- 2x LEDs (GP I/O)
- 2x SMA connectors (GP I/O)
- RS-485
- CAN FD
- I2C Power Monitor
- I2C IO Expander
- JTAG Connector
- Fan Connector
- Battery holder
- PMOD connector
- Industrial Temperature Grade Components
- 1x 10G SFP[1]
- M2 Slot[1][2]
- Mini PCIe Slot[1][2]
- 3x USB 2.0[1][2]
- 1x USB 3.0[1][2]

[1] Carrier additional features not mounted in all versions
[2] Multiplexed functionalities (a or b):
a: M2 (PCIe x1 / x2 o SATA) + 3x USB + mini PCIe
b: Mini PCIe x1 + USB 3.0

Embedded Software





SoC-e Portable Tools

In order to simplify the integration and the use of IP technology, SoC-e has developed a portfolio of portable software solutions. This portability allows implementations on reconfigurable SoC platforms, embedded CPUs or on PC systems. The following list summarizes the software modules that integrate the **SoC-e Portable Tools**:

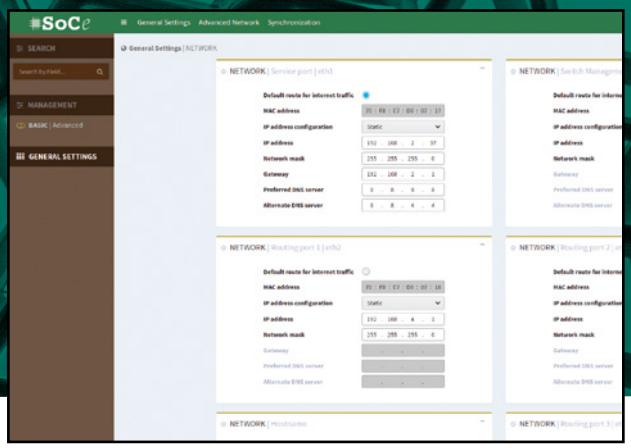
- Switch Management API
- SNMP Switch Management module
- WEB Switch Management module
- Network supervision module
- PTP software stack
- RSTP software stack
- IGMP snooping software stack
- MLD snooping software stack
- 802.1X software for authentication

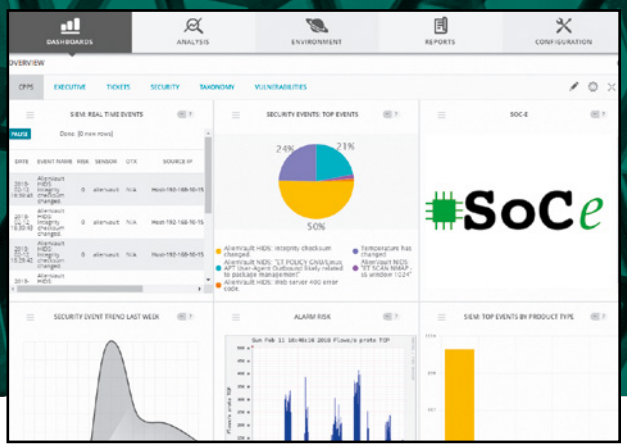
RSTP Posix-compliant Software Stack

SoC-e **RSTPdstack** is a portable C language, POSIX compatible, which implements RSTP processing according to the IEEE802.1D-2004 standard. The integration on Unix or VxWorks OS systems is straightforward. It can be used in combination with SoC-e MES IP or with other switches able to handle BDPU frames.

Key Features:

- It implements IEEE 802.1D standard and processes all RSTP Tasks such as:
  - Reception and transmission of BPDUs
  - Identification of Physical Link status change
  - Management of timeout
  - Changes in the bridge parameters and in switch's ports status
  - Switch's MAC table clearing





SoC-e Layer-3 Routing Package

The complexity of current networks demands going beyond Layer-2 Switching. SoC-e **Layer-3 Routing Package (L3RP)** is a supported software package for Linux that can take benefit for SoC-e networking IP cores or run in full software Linux based embedded system. L3RP is focused on implementing the most usual functions for a low-latency Layer-3 switch.

Key Features:

- Static Routing
- Dynamic Routing (BGP, OSPF)
- Multicast IP routing
- IPv4 & IPv6
- DHCP Server & Client
- NAT
- Firewall
- VPN

IEC 62351-9 Stack: Key Management for Substation Automation Systems

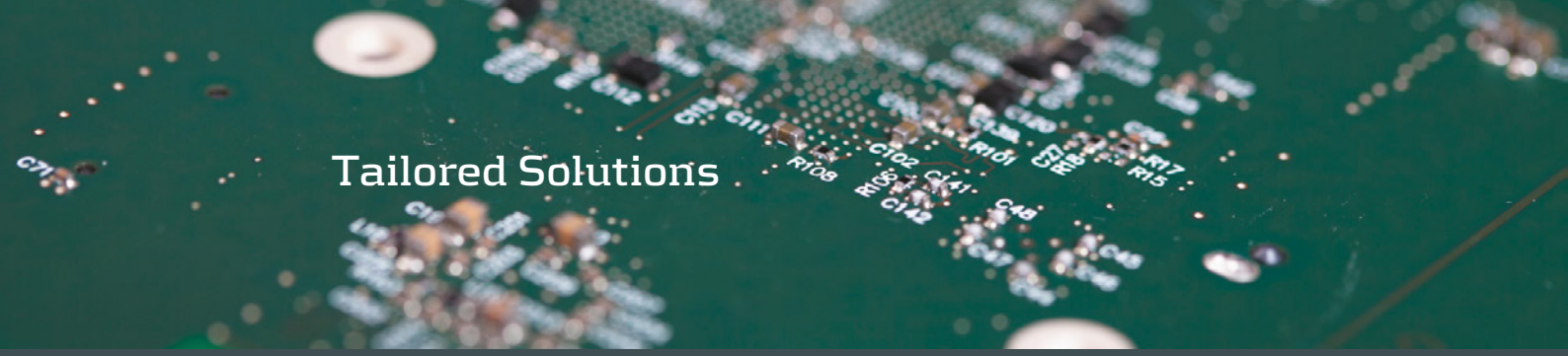
The early implementations of secure networks in unattended critical systems have faced a common challenge: how to manage and distribute properly the security keys. These OT networks are composed of heterogeneous embedded devices that should be potential destination of security keys if secure control messages need to be used by them.

The electric sector demands an adequate Key Management scheme that addresses the specific requirements of this sector. Recently, IEC has released the IEC 62351-9 standard. It specifies how the security keys and certifies need to be managed and distributed.

SoC-e has developed The **IEC 662351-9 Stack** software package that comprises all the modules required to implement IEC 62351-9 standard in an Embedded System. This package supports SoC-e Substation Automation Systems Crypto-core IP providing all the security keys required for secure critical control traffic.

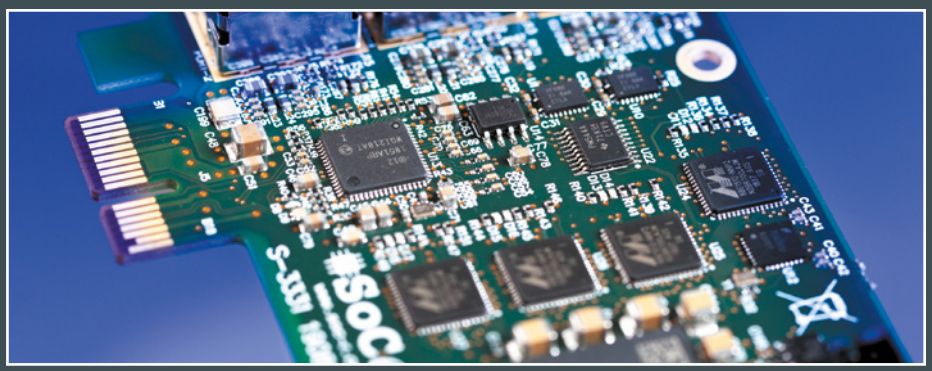
Key Features:

- TPM security IC root-of-trust support
  - Asymmetric Key Manager (AKM) module to manage:
    - Public Key Infrastructure (PKI)
    - Inventory and equipment enrolment
    - Certificates and signatures
- Symmetric Key Manager (SKM) module to manage:
  - Key interchange with Key Distribution Center Server (KDC)
  - IEC GDOI Server
- Autonomous key management for IEC 62351-6 SAS-core IP to secure GOOSE and SMV frames



Tailored Solutions

SoC-e engineers accumulate thousands of man-hours applied to the design and validation of complex FPGA and SoC based designs. These capabilities have positioned SoC-e as a trustable partner for turn-key projects focused on Industry and Aerospace sectors. The scope of these projects can vary from IP integration to full board and embedded system design.



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